Characterization of dielectric films on glass for the semiconductor 3D packaging process

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Characterization of film homogeneity and mechanical strength of the film itself are important aspects in engineering materials for back-end of line (BEOL) semiconductor processes [1]. It is a challenge to optimize such materials both for low density and for a mechanically strong structure. In terms of device integration, thickness and composition change must be minimized during high temperature process steps [2]. These factors are especially pronounced in case of bonded wafers for 3D device structures. Such stacked plates consist of Si and glass wafers molded to each other.

The bow of the constituing glass wafer can be engineered by depositing stressful SiO2 which can be modified depending on the conditions of the deposition steps, type of precursors, or type of deposition tool. Since glass exhibits half of the modulus of Si, it can easily respond to a stressful film deposited on it. With the SiO2 stress as well as variation in thickness, the amount of bow can be calculated to be engineered on the glass that would even out the total bow when these are used as carriers.

Such characteristic samples are measured, tendencies and conclusions are drawn and will be presented.

Keywords: Si wafer; porous low-k; spectroscopic ellipsometry, ellipsometric porosimetry

References

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