Delamination and transfer of wafer-scale single-crystalline monolayer graphene from SiC substrate

J. Huhtasaari[1],J.J. Palakulam[1], A. Salha[1], P. Hyldgaard[1], E. Schröder[1],M.H. Berntsen[2], O. Tjernberg[2], M. Shah[3],R. Martinez-Duarte[3], H. He[4], J. Hofmann[5,6],T. Bauch[1], N. Shetty[1], S. Lara-Avila[1],

[1]Department of Microtechnology and Nanoscience, Chalmers University of Technology (Sweden)
[2]Department of Applied Physics, KTH Royal Institute of Technology (Sweden)
[3]Department of Mechanical Engineering, Clemson University (USA)
[4]RISE-Research Institutes of Sweden (Sweden)
[5]Department of Physics, Gothenburg University (Sweden)
[6]Nordita, Stockholm University and KTH Royal Institute of Technology (Sweden)

Producing large-area single-crystalline graphene is key to realizing its full potential in advanced applications, including twistronics. Yet, controlling graphene growth kinetics to avoid grain boundaries or multilayer growth remains challenging.

Here[1], we demonstrate single-crystalline graphene free from multilayer domains via one-step delamination of epitaxial graphene from silicon carbide(SiC).This is enabled by a specific surface reconstruction of 4H-SiC(0001) achieved in our growth conditions. High crystalline quality is confirmed by the observation of the half-integer quantum Hall effect – the hallmark of monolayer graphene– in near cm-sized crystals. The scalability of our process, explored with 4”-inch wafers, represents an advance toward large-scale integration of high-performance graphene applications.

References:
[1] Huhtasaari, J. *et al.* Wafer-Scale Single-Crystalline Monolayer Graphene. arXiv:2512.00394v1 (2025).

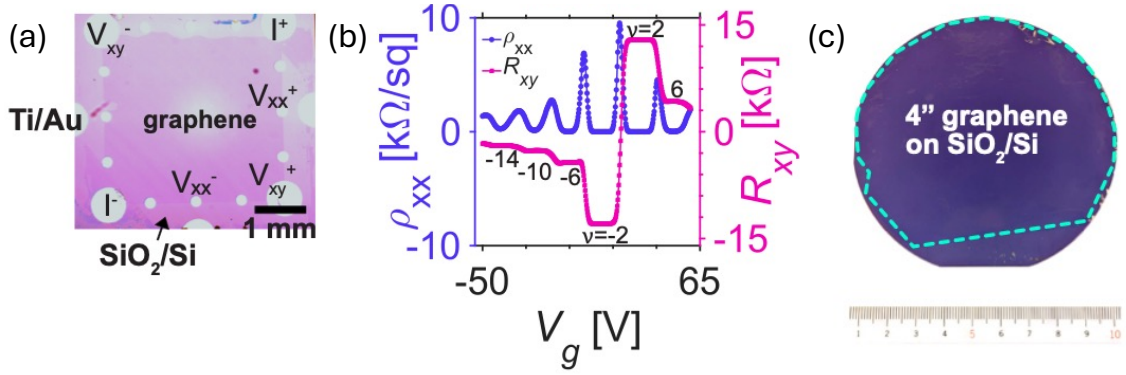

Fig. 1: Delamination and transfer of wafer-scale epitaxial graphene. (a) Large-area device with silver-transferred graphene on SiO2/Si.(b) Half-integer QHE at B=14 T, T=2 K in the large-area device. (c) 4-inch-sized graphene transferred from SiC to a 4 inch SiO_2/Si wafer.