A STUDY OF THE ELECTRONIC STRUCTURE OF ENGINEERED SOI MATERIAL

Prabhava S. N. Barimar, Jing Li, Borislav Naydenov and John J. Boland

School of Chemistry, Centre for Research on Adaptive Nanostructures and Nanodevices, Trinity College Dublin, Dublin 2, Ireland

The extreme demand for the miniaturization and increased performance of electronic devices have led to a search for low dimension, high performance and reliable materials. Silicon has been the preferred choice for decades. Silicon-on-insulator (SOI) consists of a thin Si layer known as the device layer, usually several tens of nanometres in thickness, bonded to a bulk Si wafer with an intermediate insulating oxide layer. When the silicon device layer is very thin, the effective number of atoms contributing to its physical properties are finite and small compared to the bulk. This leads to new electronic, mechanical and thermodynamic phenomena [1]. In order to study the confinement of electrons in SOI, engineered SOI structures were characterized with low-temperature scanning-tunnelling-microscopy (STM) and spectroscopy (STS).

SOIs were cleaned and thinned using plasma techniques [2] and patterned using electron beam lithography. Various scanning tunneling spectroscopic techniques such as field emission [3] and variable height spectroscopy [4] were used to study the varying density of states (DOS) of SOI structures. Significant variation in LDOS were observed for the engineered SOIs. Interestingly, apart from the effects due to low dimension of the structures, parameters such as doping concentration and annealing affects the STM and STS measurements significantly [5]. Further, using electrical measurements and kelvin probe force microscopy (KPFM) we have been able to distinguish and understand these effects. In this work we demonstrate the influence of dopant concentration and quantum confinement in SOI structures.

Keywords: Silicon-on-Insulator (SOI); Scanning tunneling microscopy (STM); Scanning tunneling spectroscopy (STS); Local density of states (LDOS);

References

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