your title please

name, lastname of First author · name, lastname of second author ·

Abstract your abstract

Keywords Configuration · FPGA · Opimaziation

1 Introduction

your content

2 Existing Methods and Tools

> **for all** $i \in I$ **do**
> $IP\_i\_is\_added \leftarrow$ false
>   **for all** $m \in M$ **do**
> $j \leftarrow$ IP, where IP $\in m$
> $i\_in\_m \leftarrow$ true
>   **for all** $c \in C$ **do**
>   **if** $i \in c$ xor $j \in c$ **then**
> $i\_in\_m \leftarrow$ false
>   **end if**
>   **end for**
>   **if** $i\_in\_m =$ true **then**
> $m \leftarrow m \cup \{$IP $i\}$
> $IP\_i\_is\_added \leftarrow$ true
>   **end if**
>   **end for**
>   **if** $IP\_i\_is\_added =$ false **then**
> $M \leftarrow M \cup \{$new module $m\}$
> $m \leftarrow m \cup \{$IP $i\}$
>   **end if**
> **end for**
> Output: M

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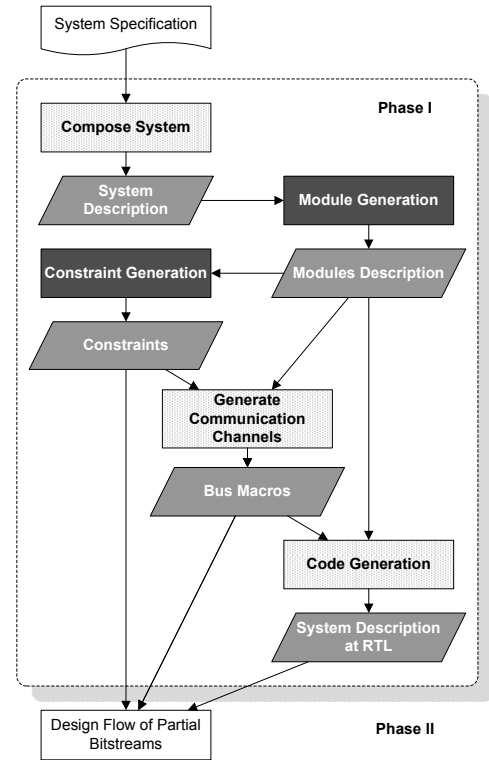
Fig. 1 Design Flow

2.1 example

content

k_s source configuration
k_t target configuration
p probability

$$f(C) \cdot \sum_{r=(k_s,k_t,p)\in R} t_r(r) \cdot P(k_s) \cdot p \tag{1}$$

IP size in CLBs	70	60	55
System size in CLBs	910	780	715
change rate in CLBs	134.17	115.00	68.75
change rate in percent	20.96%	17.96%	10.74%
number of slots	5	5	6

Table 1 Test results for the example

2.2 table

n process, then, facilitates the efficient and effective prototyping of IP based dynamic reconfigurable systems.