Stressor Films for Enhanced Transistor Performance

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1 Introduction

Straining the silicon in the transistor channel by applying mechanical stress is one of the key technologies to improve the transistor performance, namely the computing power per watt consumed electrical power. In current technology nodes, strained nitride liners are used to strain the gate area of the transistor including the conductive channel. We present recent results on improving the nitride liners, searching for alternative liner materials and on simulation of metallization process integration which are the outcome of a joint research effort between GLOBALFOUNDRIES Dresden and the Center for Microtechnologies at CUT within the CoolTrans project.

2 Improved tensile stress levels in silicon nitride liners by UV cure processes

High tensile strained silicon nitride films are one approach for stressor cap liners to improve NMOS transistor performance. A post deposition treatment under ultraviolet radiation is one way for increasing the tensile stress. This so-called UV cure leads to desorption of hydrogen and to an enhanced cross-linking due to the high energetic ultraviolet waves. As a result of this process, films are shrinking and thus have a higher density along with a higher tensile stress. In our investigations we focused on the impact of UV curing on the chemical bonding characteristics and changes in stress of differently PECVD deposited silicon nitride films. To analyze structural changes, especially modifications in Si-H and N-H bonding characteristics we used an advanced Fourier Transform Infrared Spectroscopy (FTIR) analysis.

It could be shown, that thermal assisted UV curing changes the bonding structure differently, dependent on the chemical network after deposition. With these advanced techniques films of 50 nm thickness and a tensile stress of up to 1.4 GPa could be produced.

3 Diamond-like carbon (DLC) as a new compressive stress liner material

Another approach for performance improvement is the deposition of high compressive strained diamond like carbon (DLC) on top of PMOS transistor structures. These materials are usually used as hard coatings, but up to now not in microelectronic applications. Naturally these films are a compound of sp² (Diamond) and sp³ (Graphite) bonded carbon with some amount of hydrogen and stand for high compressive intrinsic stress.

In our studies we investigated a parallel plate plasma enhanced CVD process with two different precursors and mixtures of them. Within our experiments we were able to produce films with an intrinsic stress of -3.5 GPa.

Fig. 1: Stress of UV cured silicon nitride films produced by varying the SiH₄ to NH₃ ratio.

Fig. 2: Stress of DLC films deposited with different electrode distances for different gas mixtures.
Simulation of the impact of strained contacts on stress liner performance

Stress induced by so-called stress liner materials, currently being silicon nitride, is only one of many contributions to the total stress accumulated in the transistor channel. Since direct strain measurements in the channel are still a scientific challenge, at the moment simulations are the only way to study, how stress from different sources will enter into the channel.

Contact materials such as tungsten are known to show high levels of tensile strain. In addition, processes for metallization of the source, drain and gate contacts include etching of the nitride liner and thus the stress in the liner will be relaxed in these areas. Due to the close proximity of the contacts to the transistor channel, all these effects will have a drastic influence on the stress level in the channel and thus on electron or hole mobility.

Simulations of strained transistors have been performed using Synopsys Sentaurus TCAD. Simulated process steps follow data provided by GLOBALFOUNDRIES (45 nm node). Full transistor structures including all processes involving stress formation, such as nitride liner deposition and metallization are modeled using Synopsys Sentaurus Process. Device simulations using Synopsys Sentaurus Device were used to compute current changes in the channel.

Figure 3 shows the model system consisting of 45 nm transistors including tungsten contacts in the source/drain area. The structure is derived from TEM cross sections of real 45 nm transistors provided by GLOBALFOUNDRIES. In the present study we focus on the role of the different stress contributions from the liner and from the strained contact metal. The contact stress was varied while the liner stress was fixed and vice versa. Results are shown in figure 4. While for the NMOS structure (Fig. 4a) the two contributions act in reverse direction, for the PMOS structure (Fig. 4b) the effect of the two stress sources will add up. In conclusion, best electron mobility is given for tensile strain in the contact. Hole mobility is optimum for an unstrained contact. The reason for the different behavior of electrons and holes is given by a different response of their mobility to strain, where electron mobility is improved by compressive strain in the channel, while the hole mobility favors from tensile strain.

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