Design, Fabrication, and Characterization of Ultralow Current Operational-Amplifier in the Weak Inversion Mode in XFAB-XT018 Technology

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***Abstract*—A 1.8V, 932 nA, rail-to-rail CMOS operational amplifier operating in the weak inversion regime in order to amplify the output signal of an air pressure sensor is presented. The two main parts of the ASIC are the beta-multiplier current source and the two stage amplifier. The layout has been drawn considering the matching techniques and the chip was fabricated and further characterized and measured.**

Keywords—XT018 Technology, Operational Amplifier, Weak Inversion, MOSFET, low power

I. INTRODUCTION

In today's world the degree of integration is becoming more and more important. A low power amplifier within the development of an integrated ultra-low-pressure sensor (output ranging from ten to few hundred Pascal) was designed. The power to this sensor is provided by an RFID field. To reduce losses the power consumption should be minimal. Since the op-amp consumes a big part of the available energy and bandwidth is of low importance in this application, using techniques such as weak inversion to reduce this power consumption is beneficial. It is also worth noting that the maximum transconductance-to-current ratio in weak inversion gives a very large DC gain to each stage [1]. The most common region in which the MOS devices operate is the active region. Within this region one can bias a MOS transistor to the strong inversion, the moderate inversion, or the weak inversion region. By low currents and gate-to-source voltages near to the threshold voltage the number of carriers that exist in the channel are quite low and; therefore, the diffusion current dominates the drain current and the device works as a Bipolar Junction Transistor, as the gate-to-source voltage goes higher and the amount of current to which the transistor is biased increases, the device enters the moderate inversion region and finally the strong inversion region where the drift current is the main current of the transistor.

II. CIRCUIT ARCHITECTURE

A. Weak Inversion

In real MOSFETs, the drain current is found to be nonzero for values of V_{GS} lower than V_T. In other words the subthreshold drain current can be found for slightly negative to slightly positive effective gate-to-source voltages (around 20 mV), defined as $V_{eff} = V_{GS} - V_T$ where V_T is the threshold voltage. This nonzero current is regarded as the subthreshold current.
The subthreshold current which is given by eq(1) has a hyperbolic relation with the gate-to-source voltage and does not follow the basic model reported in [2] . Since the current in the weak inversion region is a diffusion current, the MOSFET is said to be acting rather as a Bipolar Junction transistor where the source acts as the emitter, the substrate as the base, and the drain as the collector [3]. This diffusion current is given by:

$$I_D = \frac{W}{L} I_0 \exp\left(q \frac{V_{GS}}{nkT}\right) \qquad (1)$$

Where I_D is the drain current, W is the channel width, L is the channel length, V_{GS} is the applied gate to source voltage, and I_0 and n are determined by experimental results.

B. Design Process

In this work, long channel devices were used in order to achieve higher voltage gains due to reduced channel length modulation effects and higher output resistances.
Moreover, because of the larger gate areas, the threshold voltage and the transconductance mismatch reduces. The weak inversion regime can be easily applied to the wide channel devices at the differential input stage [4].
For each transistor a minimum length of 3 µm was considered which led to higher voltage gains, less threshold voltage and lower transconductance mismatch. The transistors used in this ASIC are the "ne" and "pe" MOSFET transistors in the technology of XT018 (XFAB $0.18\mu m$) which operate under 1.8V supply voltage. In order to avoid matching issues a common centroid layout was used and using the folding technique a number of $m \geq 2$ was chosen for each transistor. Specifically since the input transistors of the differential stage have to be highly matched, an $m = 4$ and large widths were chosen for them. The characteristics of these MOSFETs are shown in Table 1. For the compensation capacitors "cmm4t" capacitors were used. These capacitors are single MIM capacitors between metal3 and metaltop. The fabricated op-amp chip could be observed in Figure 1.

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III. EXPERIMENTAL RESULTS

The characteristics of the op-amp were measured using a wafer prober. A total number of 59 dies along a 200 mm wafer were measured. The mean value of the results are shown in Table 2.

Table 1. Characteristics of the transistors used in the ASIC.

Parameter	ne	pe
V_{bias}	1.8 V	1.8 V
V_{th}	0.56 V	-0.7 V
K_p	256 $\frac{\mu A}{V^2}$	52 $\frac{\mu A}{V^2}$
λwi	0.02 V^{-1}	0.02 V^{-1}

Table 2. Mean measured values

Measured Parameter	Mean measured values
DC gain	35 dB
Output offset voltage	52.4 mV
Input offset voltage	0.9 mV
Power Dissipation	1.694 μW
PSRR	88 dB
Rinp	160 GΩ
Rinn	1.736 KΩ
Output Voltage Swing	178.4 mV
Gain Bandwidth Product	16200 Hz to 23000 Hz
Phase Margin	56 to 63

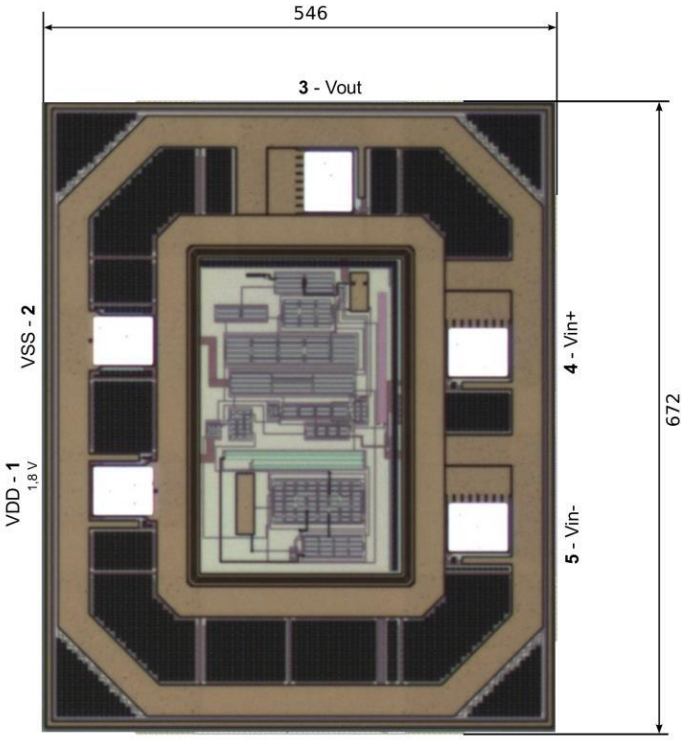

Figure 1. The photo of the fabricated op-amp chip by microscope. The sizes in the picture are in micrometers.

Rinp and Rinn are the resistances seen from the positive and negative input pins of the op-amp, respectively. A feedback is applied to the negative input pin of the op-amp. This explains the different values for Rinn and Rinp.

The currents provided by the temperature compensated bandgap reference to the second stage of the amplifier were also measured in different temperatures. The measurements were made on wafer level and the output current of the bandgap reference was measured over 9 temperatures between -30°C to 125°C A diagram of this current over different temperatures and applied supply voltages could be observed in Figure 2. It can be seen from this picture that in the optimal supply voltage (1.8V) the current has a good stability over temperature change. Moreover, the current produced for the amplifier second stage from the current source over 59 dies in room temperature is shown in a wafermap in Figure 3 where we can see a good stability of the provided current over 59 dies throughout the wafer.

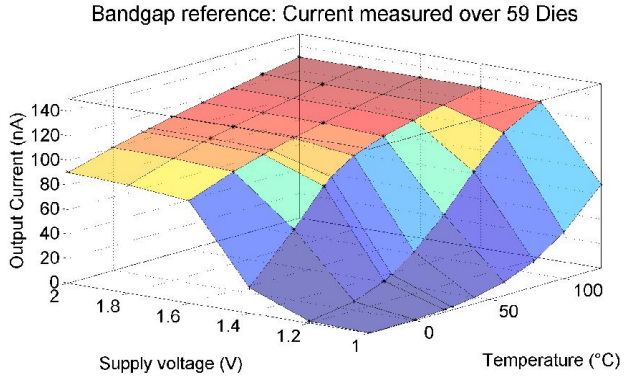

Figure 2. Current provided by the current reference to the second stage of the op-amp.

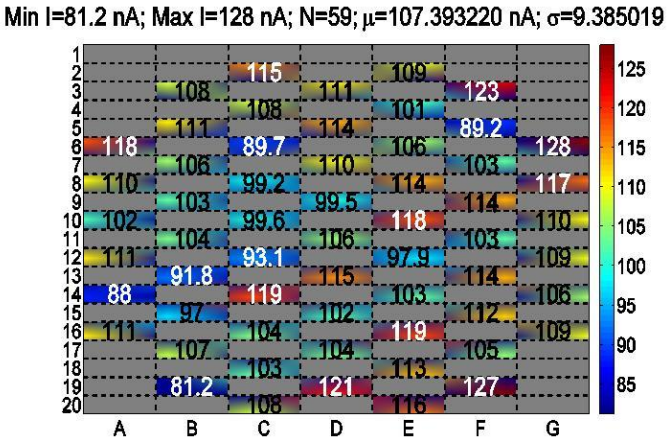

Figure 3. Wafermap of currents provided by the bandgap reference to the second stage in 59 different dies.

In this study matching techniques such as using dummy gates were applied. Transistors that must achieve moderate or precise current matching should use dummy gates to ensure uniform etching. If such a technique of dummy transistors would not be applied a current mismatch of 1% or more could occur [5]. In case of weak inversion this could change the operating point of the circuit significantly. Therefore, matching techniques were taken into consideration in designing this weak inversion operational amplifier in order to avoid such effects. The current consumption wafermap could be observed in Figure 4. Furthermore, DC gain wafermap under a supply voltage of 1.8 V is illustrated in Figure 5. It could be seen that very small variation over the DC gain and current consumption is observed throughout the 59 dies in the wafer. These small variations over the wafer are direct result of following the matching rules in the layout design.

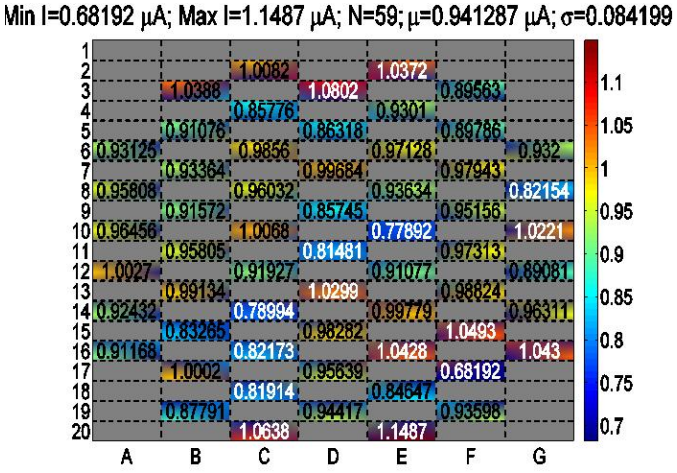

Figure 4. Wafermap of the current consumption of the Weak Inversion op-amp.

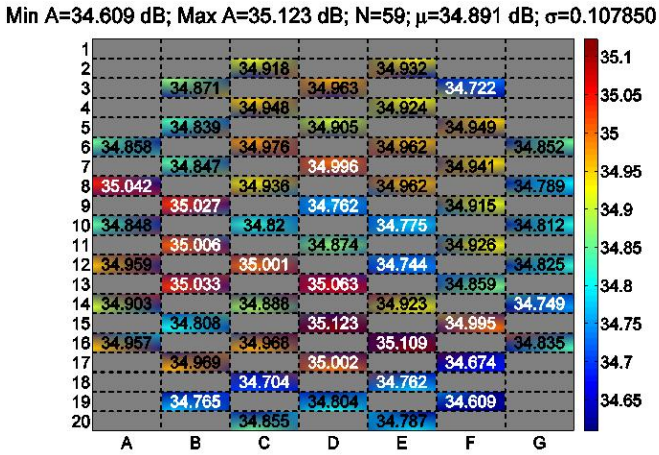

Figure 5. Wafermap of the DC gain by a supply voltage of 1.8V.

IV. Conclusion

The operation of MOSFETs in weak inversion mode is exploited in order to design a rail-to-rail operational amplifier that consumes a very small amount of power (1.694 μW). The use of weak inversion makes the saturation voltage very low and this allows an output signal with almost no distortion with a peak-to-peak amplitude very near to the supply voltage. The ASIC is composed of two main parts, the temperature compensated beta multiplier current source and the two-stage amplifier. The temperature compensated beta multiplier current source exploits from a negative temperature coefficient resistance in order to compensate the effects of elevated temperatures and gives the ASIC a good stability against temperature variation in the range of -40 °C to 125 °C. The beta multiplier also sources small enough currents to the amplifier stages to guarantee the operation of amplifier stage transistors in the weak inversion region. With a total current consumption of 932 nA the op-amp is consuming far less current than conventional low voltage op-amps like AD8515 that consumes a current in a range of 325 to 450 uA. Such a low power consumption with the suitable and stable small signal behavior (DC gain of 35 dB and a phase margin of 63 degrees) makes it a very suitable option for energy efficient and standalone systems where the bandwidth and speed is not an issue and low power consumption is of high importance.

V. Acknowledgment

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