SoC Low Differential Air Pressure Sensor

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1 Introduction

In air filters a major challenge is to monitor their wear. In the beginning of their lifetime the filtering is not optimal. But with time the particles clog the holes and increase the filtering effect. The filter is best at the end of the lifetime. At the same time the filter clogs faster because of his higher effectiveness. This leads to the need to monitor the wear of the filter. Easiest is measuring the time of use under the assumption of a constant particle content in the air. This is inaccurate and often the filters are replaced to early or when they are already completely clogged. Measuring the pressure difference before and behind the filter gives more accurate results. This approach is used in complex industry systems. For small filters those systems are too large and expensive. The goal is the development of a sensor, which is able to measure the pressure difference occurring on filters.

This application leads to the following requirements:

- Pressure Range from 0.1 to 5 mBar with a resolution of 0.05 mBar
- Low cost
- Integrated into the filter, thus small size
- Power and signals over RFID, thus low power and high noise immunity
- A measure time up to one second is acceptable

Image [1] shows the system, which consists out of two ASICs. One of them contains the sensor and analogue signal pre-processing. This is necessary for a sufficient signal to noise ratio on the bond wires to the second ASIC. The evaluation ASIC converts the signals to digital values, does digital signal processing and handles the RFID communication. This paper will cover the sensor ASIC only.

2 Membrane

The central element in a pressure sensor is the transducer converting the pressure to electrical parameters. This sensor uses a common approach of a membrane with piezoresistors. The conversion happens in two steps. First the pressure difference

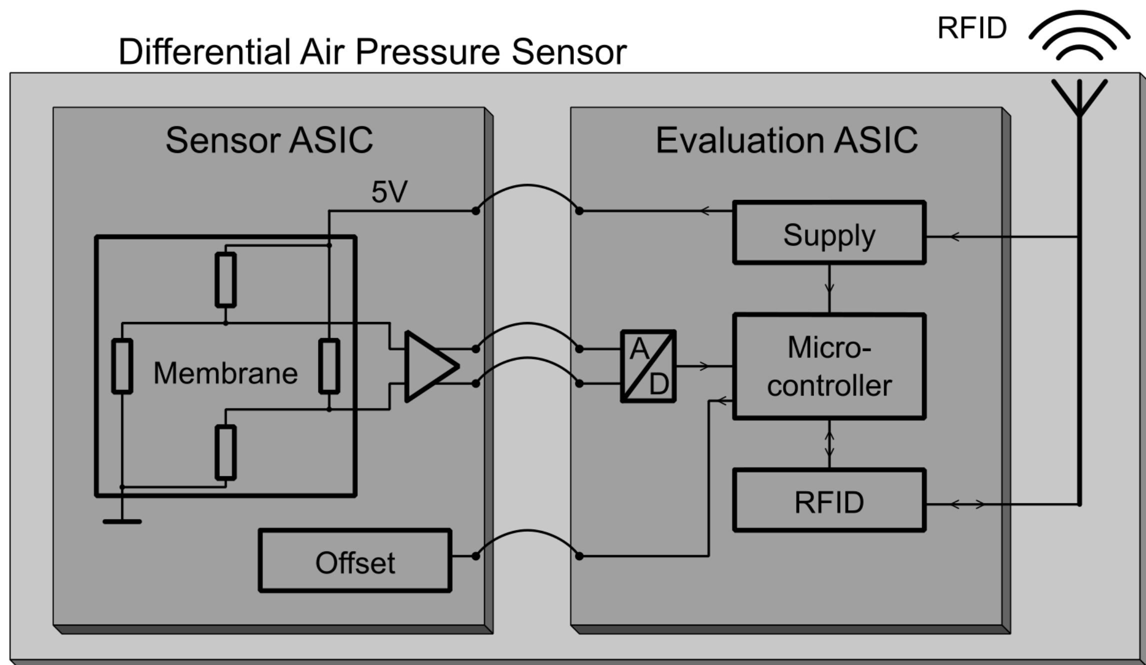

Fig. 1: Schematic overview of the measurement system
to detect the wear of air filters

results in a deformation of the membrane and thus stress in the edges. In the second step the stress changes the values of resistors by the piezo effect. This leads to a change in current or voltage at the resistors. These electrical parameters will be processed further.

For the measurement of the very small differential pressure of only 5 mBar the membrane has to have a high sensitivity. A common parameter for a membrane with Wheatstone bridge is the sensitivity given in millivolt per Volt bridge supply voltage per Bar differential pressure. The sensitivity is essentially defined by the membrane and independent of the size of the resistors. Inconvenient layout of the resistors may reduce the sensitivity. The sensitivity has been defined to 160 mV/V/Bar to get appropriate output signals as extrapolation from data's shown in [2]. The output voltage then will be 40 µV for a step of 0.05 mBar and 4 mV full scale. This shows the need for on-chip signal amplification. Otherwise the signal to noise ratio would be too small for transmission over bond wires.

To reach the comparably high sensitivity together with the ability of integrated CMOS circuitry a modified 180 nm Technology from X-FAB Semiconductor Foundries AG is deployed. It is based on the new XT018 node and extended by etchings to produce the membrane. The process uses a SOI Wafer. First the entire CMOS circuits are produced. This includes a wide variety of transistors, resistive and capacitive devices and four metal layers for wiring. Following the membrane is etched. To do so the bulk silicon is removed with a dry etching. Compared to a KOH etching less die area is necessary as fig. [4] shows and reduces therefore costs. The etching stops on the

buried oxide layer, which is removed subsequent. At the top a second dry etching removes the intermetal isolators down to the lowest metal MET1. A plate in MET1 covers the membrane and stops the etching. The metal is removed afterwards. Figure [3] shows the remaining layer stack. Figure [4] and [5] show a cut through the fabricated ASIC.

The membrane is comparably thin to reach the high sensitivity. The remaining silicon layer measures 3500 nm to which the silicon dioxide adds approximately 1000 nm. The membrane dimensions have been extrapolated to 800 by 800 µm to reach the desired sensitivity.

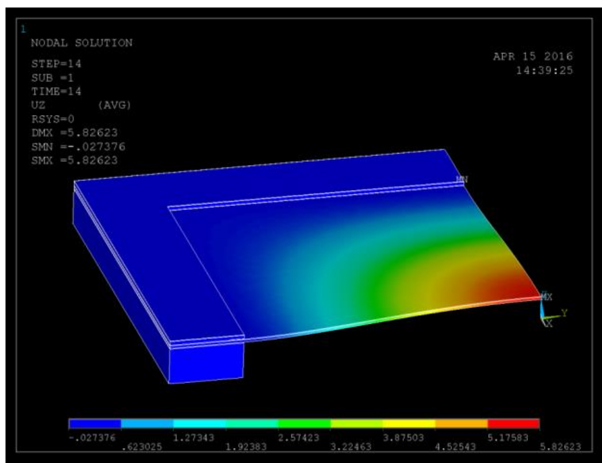

Fig. 2: FEM simulation of the membrane with respect to the technology

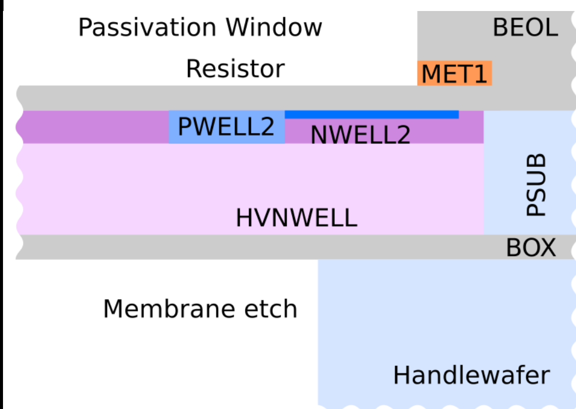

Fig. 3: schematic drawing of the technology

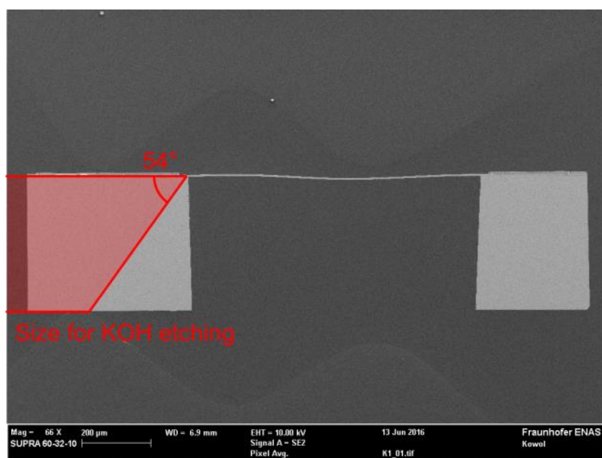

Fig. 4: Polished Chip along the long edge (1500 µm) showing the 4.5 µm thick and 800 µm wide membrane

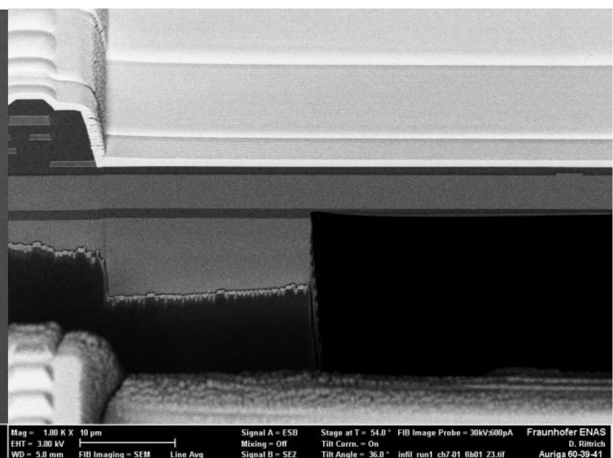

Fig. 5: FIB cut of the membrane edge.

3 Piezoresistors

A full Wheatstone bridge is deployed to convert the resulting stress in the membrane into an electrical parameter. The resistance should be high, to reduce the power consumption. On the other hand the noise of the resistor increases with its value. Out of the system design the resistance has been compromised to 40 kOhm. The piezo coefficients depend on the orientation of silicon, stress field and current flow. Therefore only resistors with p-type conduction are relevant for this design. They have high piezo coefficients if they are placed parallel or perpendicular to the stress field. In the same orientation the piezo coefficients for the n-type resistors are close to zero.

The XT018 Technology [3] contains process steps to integrate high voltage components. Thus more diffusions are available compared to a standard CMOS process. There are two different P and N well diffusions and deep N and P diffusions. The resistor is built of a P well structure with a suitable sheet resistance. It is surrounded by N well and the deep N diffusion for isolation against the substrate silicon. The resistors are placed on the edges of the membrane in the areas with the highest stress for high sensitivity. The structure is broadly shown in figure [3]. The layouts of the parallel and perpendicular resistors are matched to reduce the bridge offset to a minimum.

4 Electronics

As shown earlier, the signals from the bridge have 4 mV maximum and a resolution of 40 µV. It would be impossible to transfer this signal with 40 kOhm Output Impedance over bondwires within an RFID field into several megaohm input impedance. Signal conditioning and lowering the output impedance is essential. An instrumental amplifier will do both of it. The evaluation ASIC has an ADC with an input range of ±400 mV differential voltage around a common mode voltage. An

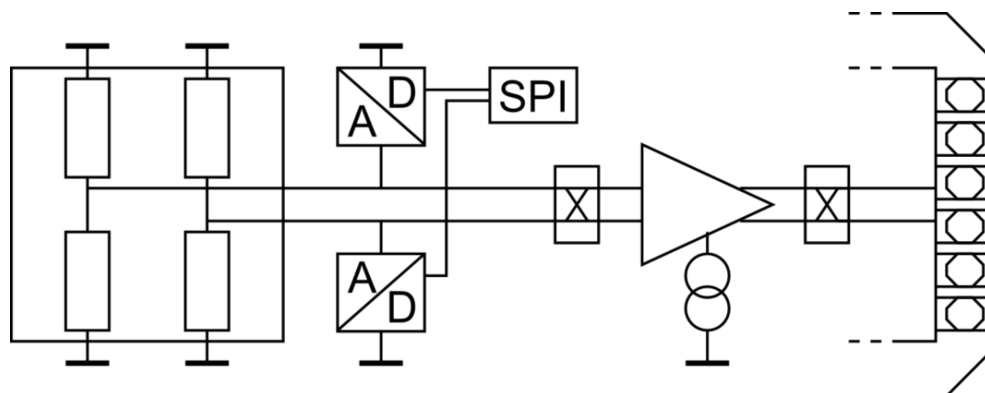

Fig. 6: Block schematic of the Sensor ASIC. Left the membrane with Wheatstone bridge to the bondpads on the right.

amplification factor of 135 will boost the 4 mV full scale output of the bridge to 540 mV for transmission. To reduce the contributed noise of the amplifier, it is implemented as a chopper amplifier. [1]

The output of the amplifier shouldn't exceed ±400 mV under all conditions. In other words the input voltage has to be smaller than ±3 mV. Considering the full scale signal is deducted there are only 2 mV left for parasitic signal changes. A major problem is the initial offset of the bridge. Small mismatches of the resistors lead to offsets much higher than 2 mV. Rough estimations led to an expected offset variation of ±100 mV. This is a multiple of the full scale output and would drive the amplifier into its limits. An offset compensation is mandatory. This is indicated in Fig. [6] by the two digital analog converters connected to the bridge outputs. Those are binary weighted current steering DACs. The outputs are set by a SPI Slave Controller. If the value is not zero, the DAC draws a current to ground. This current adds to the bridge current resulting in a lower node voltage. The offset can be compensated in two times 128 steps of 800 µV. Each step of offset compensation shifts the output roughly about 100 mV. This is enough to ensure, that the full scale output won't reach the limits of the amplifier. A full compensation of the output to zero is not necessary and would require DACs with an ENOB at the minimum 14 Bits.

5 Measurement Results

In the first preparation many different variations of membranes, resistor layouts and electronics had been implemented. All individual components had been characterized in detail. The amplifier and the offset compensation are working within the specification. As they are well known circuits a detailed description of their performance is skipped.

The measurements of the transducers show the expected dependency of the bridge voltage against the differential pressure. The results are shown in Tbl. [1] and fig. [7]. Unexpectedly the measured sensitivity is with a mean value of 400 mV/V/Bar much higher than the expected 160 mV/V/Bar. Contrastingly the worst case offset values

Sample	**Sensitivity** mV/V/Bar	**Offset** mV/V	**Nonlinearity** mV/V/Bar^2
3	409	-3,4	5524
5	410	-3,4	3134
7	294	-2,8	1698
22	349	-0,9	3196
23	377	1,2	3974
24	474	-1,4	5007
28	493	1,0	6157
Ø	**400**	**-1,4**	**4098**

Tbl. 1: Measurement results of a representative subset of the samples.

Sample	Sensitivity mV/V/Bar	Offset mV/V	Nonlinearity mV/V/Bar^2
29	567	-0,4	17948
26	673	-2,9	21823

Tbl. 2: Measurement results of samples originating from the wafer border.

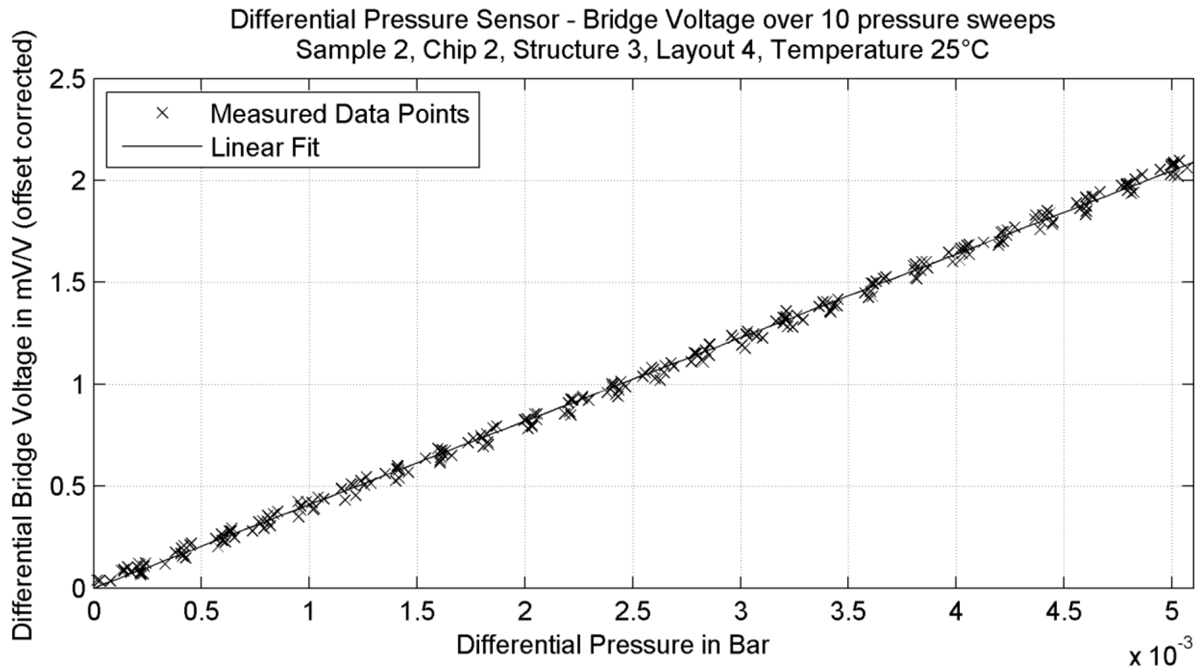

Fig. 7: Exemplary measurement result of sample 5. The pressure has been swept ten times up and down.

are below the expectation. This is a result of the layout efforts to reduce it. With a 5 V bridge supply voltage the offset ranges from -17 mV to 6 mV, whilst the offset correction is able to compensate up to ±100 mV.

Some of the measured samples showed a more nonlinear behavior. Two examples are given in Tbl. [2]. The stated nonlinearity is a factor of a quadratic equation fitted to the data. The values are nearly 5 to 10 times higher, compared to good behaving samples as in Tbl. [1]. A big influence on the parameter fluctuations is based on the placement on the wafer itself. The nearer the circuit is situated at the border of the wafer the bigger the nonlinearities are. The dependency is shown by a white light interferometer measurement in Fig [8]. It is apparent, that the initial deflection is 1 µm or 50 % higher at the border. The explanation lies in the used technology. Directly at the membrane ends the buried silicon oxide of the SOI wafer. On top of the membrane is 1 µm of silicon oxide, too. Both oxides are produced in high temperature steps and introduce a large stress between the silicon and the oxide. By removing the bulk silicon and the top layers of the back end of line, the stress releases into the membrane.

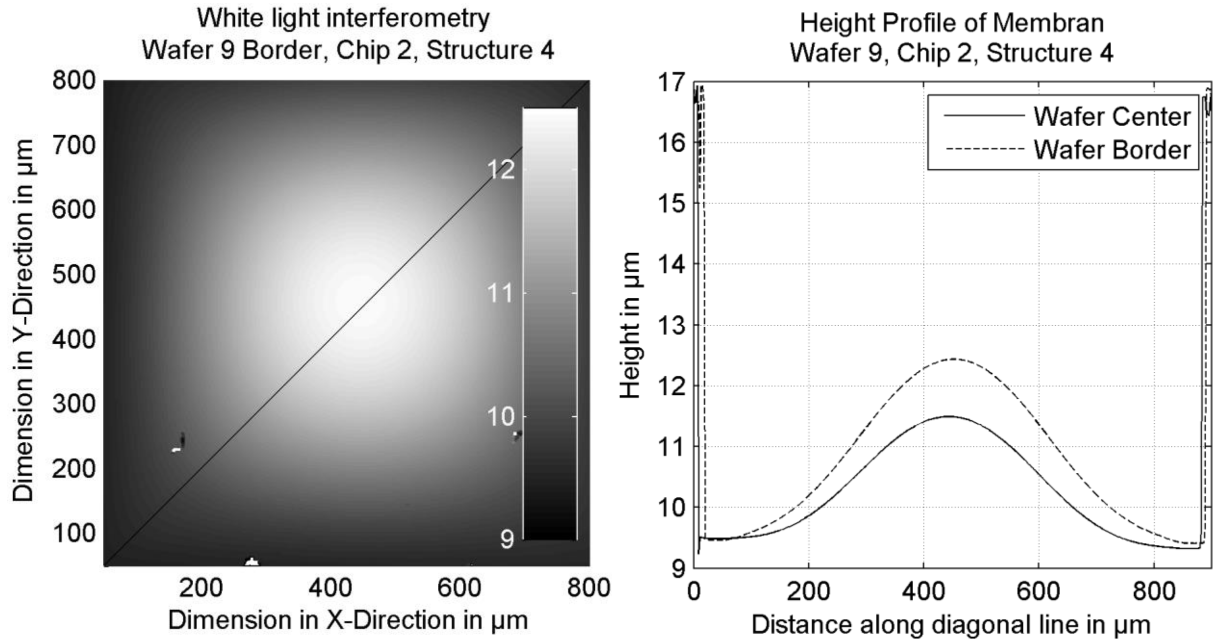

Fig. 8: Deflection of a membrane measured with white light interferometry. Left: Top view of the membrane. Right: Comparison of the deflection of a membrane at the wafer border and the wafer center.

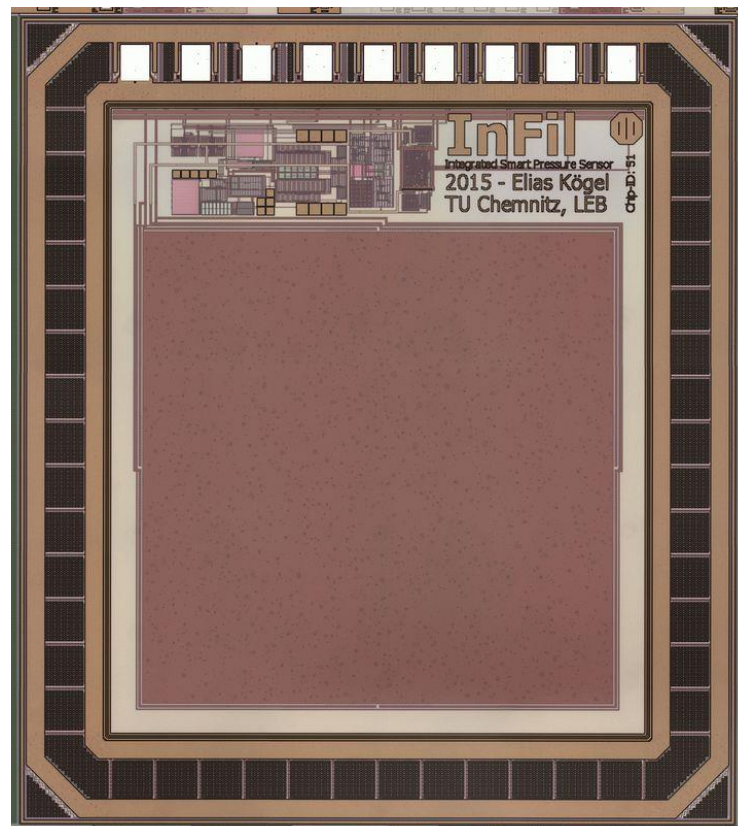

Fig. 9: Microscopy of the ASIC (1500x1300 µm)

This is an unexpected behavior resulting in a pre-stressed membrane. The higher the intrinsic stress is the more instable is the initial deflection at zero differential pressure. If the intrinsic stress increases, the buckling increases and the transfer function gets more nonlinear. At certain point the nonlinearity turn into a hysteresis. The effect increases with temperature and membrane size. A major benefit on the other hand is the much higher sensitivity as stated above.

6 Conclusion

A system has been developed to measure differential pressures as small as 5 mBar with a resolution of 0.05 mBar. The micrograph in Fig. [9] shows the full ASIC. It is a system-on-chip containing MEMS together with analogue and digital circuitry. This combination allows preprocessing of the signals for a stable transfer to the evaluation ASIC. All components have been characterised in detail. The results of the membrane are presented and show intrinsic stress in the membrane, induced by the surrounding silicon oxide layers. Due to it the membrane can have a nonlinear characteristic, whilst the sensitivity is increased. This gives the possibility to reduce the membrane size further, and therefore the costs. Meanwhile the nonlinear effects are expected to reduce, too.

A redesigned ASIC is in production at the present moment. The membrane size has been reduced down to the desired sensitivity. It is expected, that the nonlinearity due to intrinsic stress will reduce.

7 Acknowledgement

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8 References

[1] Enz, C., Temes, G.: *Circuit techniques for reducing the effects of op-amp imperfections: autozeroing, correlated double sampling, and chopper stabilization*, Proceedings of the IEEE, Institute of Electrical and Electronics Engineers (IEEE), 1996, 84, 1584-1614

[2] Heinz, S. et al.: *A monolithic integrated MEMS in a 350nm technology for filter monitoring applications*, AMA Conferences SENSOR 2013, 16th International Conference on Sensors and Measurement Technology, 14 - 16 May 2013, Nürnberg, ISBN 978-3-9813484-4-6, doi:10.5162/sensor2013/C2.3

[3] XFab Semiconductors Foundry AG: *0.18 µm Process Familiy: XT018*, http://www.xfab.com/fileadmin/X-FAB/Download_Center/Technology/Datasheet/XT018_Datasheet.pdf, 30 January 2017