High-Voltage Amplifier Design for MEMS based Switching Arrays in Wavelength-Division Multiplexing Networks.

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***Abstract*—The paper describes the design requirements of integrated high-voltage amplifiers for large MEMS based arrays which consist of electrostatically driven actuators. Such actuators are applied in optical switching arrays for cross connects in wavelength-division multiplexing (WDM) networks. Besides a new calculation approach for the efficiency of amplifier operation modes a new concept of level-shifter circuitry for switching output stages of high-voltage amplifiers is presented and compared with conventionally level-shifter circuits.**

I. Introduction

Data occurrence and the demand of network capacity are strongly increasing as a result of broadband connections and real-time data transfer in video conferences and the propagation of voice over IP. Data network capability has to be extended to meet these requirements. One solution is the application of fiber optical networks. These over-all optical networks allow a data transmission rate up to 10.000 Gbps. The operation of wavelength-division multiplexing (WDM) networks requires optical switches for cross connects of the wavelength-separated channels (lambdas). MEMS based switching arrays can perform this task [1]. High-voltage amplifiers or so called high-voltage drivers with 50, 100 or more channels just onto a sole chip are required to drive these MEMS based switching arrays. Important properties of such integrated high-voltage amplifiers are power consumption and waste heat. In particular the chip area must be small enough to facilitate the system integration with MEMS based switching arrays. Conventional smart-power circuitries don't fulfill these requirements. Therefore a search for new methods of implementation is necessary. The combination of pulse width modulation amplifiers (PWM class D type) with new, very low quiescent current consuming, high-voltage level-shifters enables the integration of hundreds or more driver channels onto a single chip. These high-voltage driver chips and the MEMS based switching arrays will be integrated as system in package for instance with "flip-chip" attachment on one motherboard [2].

II. The Electrostatic Actuator Array

In the collaborative research center "Arrays of micro-mechanical sensors and actuators" at the Chemnitz University of Technology one focus of interest are electrostatically driven actuators. Fig. 1 shows a 1-degree of freedom (1D) micro mirror with electrostatic drive. The flexible plate consists of silicon and forms the upper electrode. The surface is coated with a thin layer of aluminum and forms the mirror with the dimensions: a = 2.8 mm, b = 1.7 mm. The two back-plate electrodes are located on a glass substrate face to the mirror and consist of aluminum. The electrostatic forces initiate by high-voltage signal tilt of the mirror plate around one axis. Another type of micro mirror allows biaxial motion control (2D-micro mirror) [3].

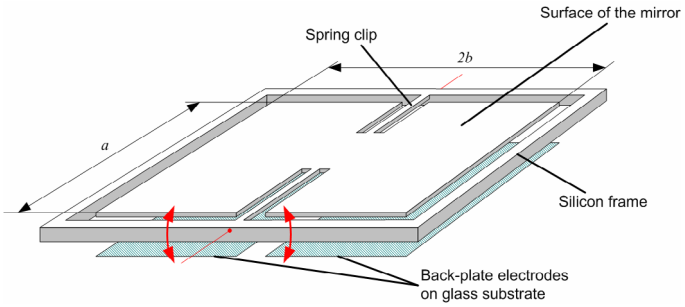

Fig. 1. Schematic of 1D-micro mirror

A MEMS based switching array consists of several arrays and each array of several micro mirrors. Loke describes an optical switching system with four 9 x 9 micro mirror arrays [4]. Fig. 2 shows a prototype of a 9 x 9 micro mirror array.

The mirror operation in an optical switching matrix requires high-voltage driver signals to adjust several tilt angles. Therefore the high-voltage driver signal must be analog or apparently analog.

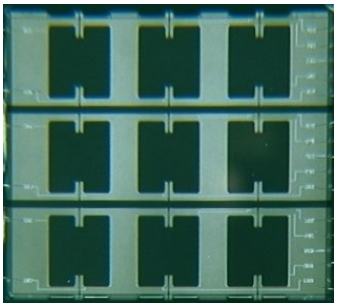

Fig. 2. Micro mirror array with 9 x 9 1D-micro mirrors (Prototype)

The electrical behavior is dominated by the capacitive component. This component consists of a variable part and a fixed part. The fixed part is eight times higher than the variable part for the actuators described in [4]. The over-all capacity C is less then 2 pF. Due to the small capacity only little energy W_E is necessary to drive electrostatic actuators. Equation 1 indicates the relation (Q .. electric charge, V .. electric voltage).

$$W_E = \int_0^V V \cdot C dV = \frac{Q^2}{2C} \tag{1}$$

Concepts of energy recovery, like in applications with piezoelectric driven actuator, are impracticable. That implies that small power consumption of the amplifier circuitry, in particular in the high-voltage output stage, represents an important demand. This is guaranteed by an efficient amplifier operation and small parasitic capacities in the physical amplifier layout.

III. Efficient Amplifier Operation

Conventionally (power-) amplifiers are classified in several operation classes in dependence of their dc operation point (OP). Common known operation class designations are class A, AB, B and class D. Thereby class A, AB and B amplifiers have a linear operation mode whereas class D amplifiers switch the output from rail to rail, controlled by pulse width modulation (PWM). For ohmic loads the power efficiency always is least at class A operation and highest at class D operation. Further classifications with characters E, F, … in the Latin alphabet are not conventional. A summary is presented by Self [5].

With capacitive loads the behavior has to be reinvestigated. Amplifiers driving capacitive loads force only reactive power on their output clamps. The power efficiency is defined as the ratio of signal power delivered to the load and the total power consumed by the system. It is calculated by averaging over the cycle duration of sinusoidal signals. The power efficiency is consequently zero in the case of capacitive loads. A new approach has to be established for efficiency calculations of amplifiers with electrostatic driven actuators. The balance of electric charge transfer per unit time should be considered. The procedure of calculation is described in [6].

The result of calculation with charge transfer approach is shown in Table I. Only the ideal behavior of operation is regarded. Therefore for the calculations ideal output stages without parasitic elements and without feedback loop were assumed. The table compares ideal class A operation with ideal class B and class D PWM operation. Fig. 3 shows exemplary the schematic of the class A output stage and the time domain behavior of voltages and currents.

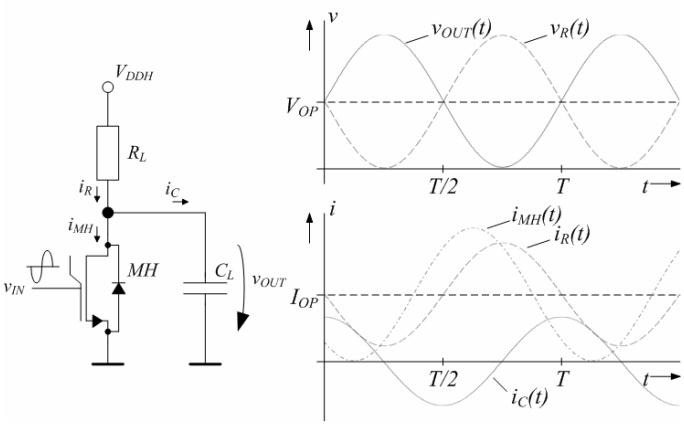

Fig. 3. Amplifier output stage with capacitive load and ideal class A operation

TABLE I
Efficiency Calculation (Charge Transfer Approach) for Amplifiers with Capactive Load

Form of control signal	Class A operation	Class B operation	Class D PWM operation
Sinusoidal	$\frac{4\hat{V}_{OUT} C_L R_L}{V_{DDH} T}$	1	$\frac{2\hat{V}_{OUT}}{V_{DDH} N_{PP}}$
Sinusoidal, Rail to Rail	$\frac{2C_L R_L}{T}$	1	$\frac{1}{N_{PP}}$
Constant value, $0.1 \cdot V_{DD}$	$\frac{C_L R_L}{9T + C_L R_L}$	No operation	$\frac{0.1}{N_{PP}}$
Constant value, $0.9 \cdot V_{DD}$	$\frac{C_L R_L}{\frac{1}{9}T + C_L R_L}$	No operation	$\frac{0.9}{N_{PP}}$

The comparison of the operation efficiencies in Table 1 reveals the expected dependence of the class A operation from modulation range and time constant of the load. Surprisingly, the class D PWM operation shows an equivalent behavior. Its efficiency depends also on the modulation range. Within every switching cycle the charge transferred to the capacitive load also will be transferred to the ground. Therefore the efficiency depends furthermore on the frequency ratio between switching signal and control signal N_{PP}, similarly to a kind of time constant. The efficiency of the class B operation is equal one at maximum. A class B operation with constant control signal and with capacitive load is impossible.

In evaluation of these efficiency calculations a combination of the class A and B operation modes for high-voltage

amplifiers with capacitive loads occurs as a logical consequence compared to class D PWM operation. A combined class A, class B (not class AB) high-voltage amplifier is demonstrated in [7].

However, the calculation doesn't respect parasitic influences. The concept of the combined class A, class B amplifier needs a feedback coupling within the high-voltage output stage, likewise a class A amplifier. This feedback loop causes an additional charge transfer and reduces the amplifiers efficiency. The concept of the class D PWM amplifier doesn't need the feedback coupling within the high-voltage stage. The principle operations are shown in the block diagram (Fig. 4).

The amplifier modulates the analog input signal to a square wave carrier frequency by variation of pulse width. The output signal (PWM_OUT) swings from one rail to the other. The complete PWM controller only consists of low-voltage devices. The low voltage PWM signal (PWM_OUT) is coupled back to the summation element. The feedback loop is an integral part of the low-voltage circuitry. The high-voltage circuitry converts the modulated square wave into a high-voltage PWM output signal (V_{OUT}) to drive the capacitive load respectively the micro mirror.

The obtainable signal transfer accuracy depends on rise and fall time of the high-voltage pulse width modulated output signal. The absolute delay time has secondary importance. But a correct balance of the delay time between high-side and low-side in the high-voltage output stage is very essential. Due to these interrelations the temperature dependence is small – a weighty factor for array applications.

The demodulation is performed by the actuator. The mechanical resonance frequency is much smaller than the carrier frequency of the amplifier. Therefore the movement of the actuator doesn't follow up the carriers swing. The low pass behavior of the actuator leads to an averaging of the high-voltage output signal and with it to an analog signal return.

These properties of class D PWM amplifiers rebut its disadvantage ascertained in the efficiency calculation. The class D PWM operation mode is favorable for electrostatically driven actuator arrays.

IV. Dynamic High-Voltage Level-Shifter

The level-shifter determines the properties of the circuitry first of all as an essential circuit element in the high-voltage switching output stage. Power and chip area consumption depend on circuit isolation technology and circuit implementation. A dielectric isolated circuit technology is indispensable for array applications. Low leakage currents, a small chip area as well as small and voltage independent isolation capacities are the significant advantages of this isolation technique [6].

Conventional level-shifter implementations consume either a lot of power or much chip area with the effect of a low switching frequency and a long delay time. A static level-shifter implementation is presented in [8]. A high-voltage differential pair with cross-coupled loads forms a voltage mirror. The advantage of this circuitry is its quasi built-in power supply to generate the second high-voltage rail for the high-voltage PMOS driver ($V_{DDH} - V_{DD}$). The disadvantage is its current consumption. The current flows from the high-voltage rail to the ground continuously, either in the left or in the right part of the differential pair. This current can not be reduced to any desired value. It determines the maximum switching frequency. Fig. 5 shows the measured voltage-time characteristics of this circuitry. Ch 4 displays the input signal with a switching frequency of 80 kHz. The value of the high-voltage rail amounts 300 V and the averaging current consumption is 160 µA. The measurement shows a high propagation delay of about 1.2 µs.

For power saving operations must be applied dynamic level-shifters. Diazzi presents a circuit design with two reciprocal switching high-voltage transistors [9]. The used pulse operation allows a short on-period of the transistors. Therefore also the current flows during a short time only. This circuit concept with its significant signal forms is represented in Fig. 6. However due to several disadvantages it is impossible to use this circuitry for array applications. The non differential operation mode increases the susceptibility to noise. The necessary clamp diodes for over-voltage protection at the nodes V_{X1} and V_{X2} reduce the performance of the circuit by parasitic capacities and thus increase the propagation delay.

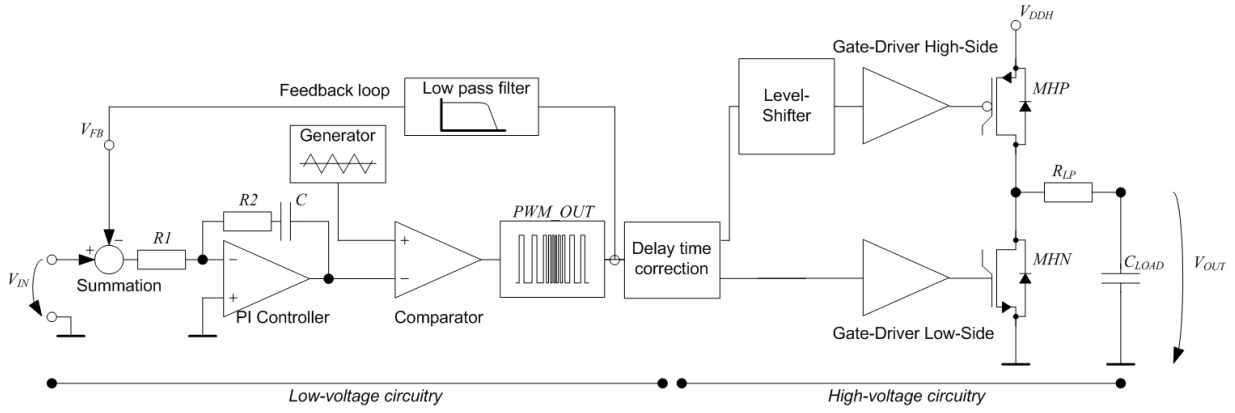

Fig. 4. Block diagram of a class D PWM high-voltage amplifier

Moreover, the required chip area increases.

Therefore a new circuitry concept had to be developed. The result, a high-voltage level-shifter with the functional principle of a charge pump, is shown in Fig. 7 [10]. This circuitry concept works without high-voltage transistors. The only high-voltage devices are the two pumping capacities. The current consumption is very small. It is determined by the load current in the enabling cycle and the periodic charge transfer between high-side and low-side. The cross-coupled inverters in the high-side perform two tasks. The first one is the latch function to solve the switching state. The second one is the over-voltage protection achieved by the substrate diodes of the transistors. Thus the required chip area is small.

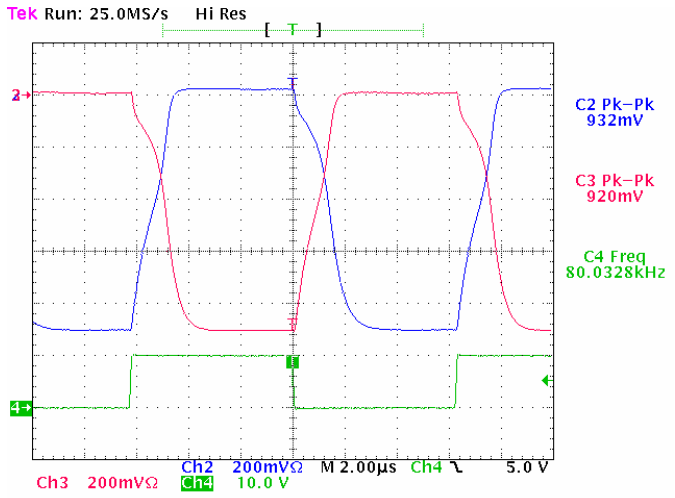

Fig. 5. Measured output signals on the static level-shifter circuit, Ch4: input signal, Ch2: non inverted output signal at high voltage rail, Ch3: inverted output signal at high-voltage rail (CH2, Ch3 measured with isolation amplifier and probe divider of 10:1)

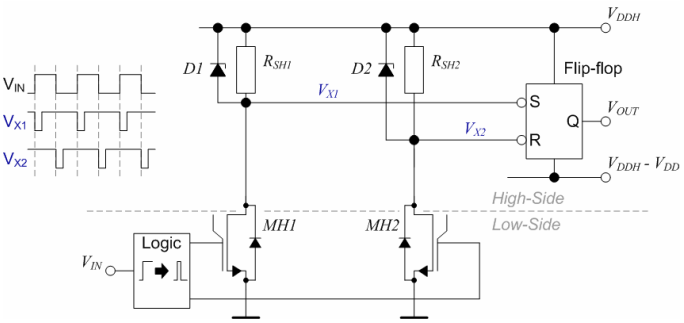

Fig. 6. Dynamic level-shifter circuitry, described in [9]

The switching-frequency and thereby the propagation delay is determined by the capacities. They can not be reduced to any desired small value. The capacities must deliver the current to overcome the change-over point of the cross-coupled inverters in the high-side. Fig. 8 and Fig. 9 show the simulated current-time characteristics. The plots represent the transfer of the rising edge over C_{SH1} (Fig. 8) and the falling edge over C_{SH2} (Fig. 9). The transistors M2 and M3 take over the currents from the capacities up to the switch-over point. Then M1 and M4 recharge the capacities.

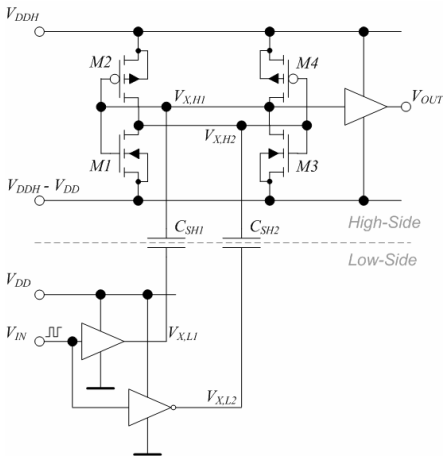

Fig. 7. Dynamic level-shifter with charge pump function

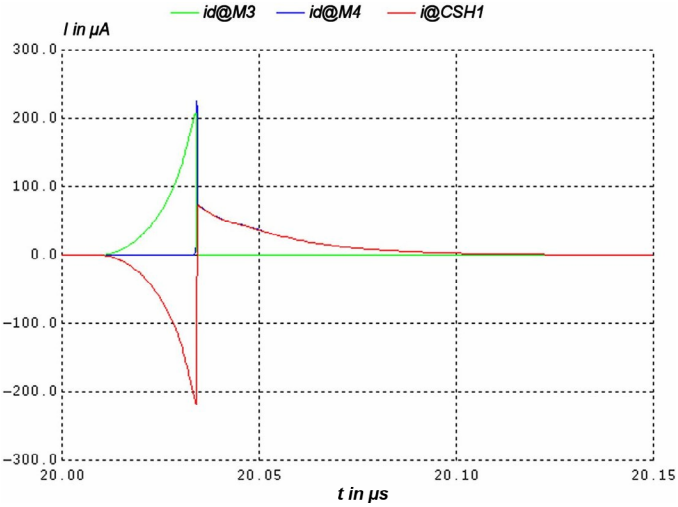

Fig. 8. Simulated current-time characteristics – rising edge

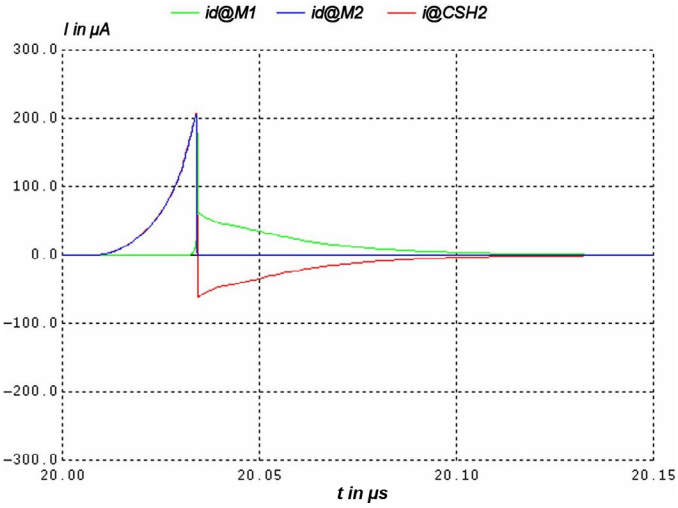

Fig. 9. Simulated current-time characteristics – falling edge

The maximum current is dependent on edge steepness caused by the driver strength of the low-side drivers. The necessary value of the capacities can be calculated with the assumption of equal NMOS and PMOS threshold voltages V_{TH}. The transistor capacities have to be neglected. Regarding to Fig. 7 the current through the both transistors, which are in active region, defines (2). Therein V_{DD} is the supply voltage of the inverters in the level-shifter high-side and β the trans-conductance parameter of the transistors.

$$I_D = \beta\left[\left(V_{DD} - V_{DS} - V_{TH}\right)V_{DS} - \frac{V_{DS}^{\,2}}{2}\right] \tag{2}$$

With the assumption that the maximum currents flow at $V_{DS} = \left(V_{DD} - V_{TH}\right)/3$ follows (3). Equation (4) defines the transferred charge, thereby the fall and rise times are equal ($t_R = t_F = t_{R,F}$).

$$I_{D,\max} = \frac{\beta}{6}\left(V_{DD} - V_{TH}\right)^2 \tag{3}$$

$$Q = \int_0^{t_{R,F}} i dt = I_{D,\max} \cdot t_{r,F} \tag{4}$$

The change-over point of the inverters should be designed to $V_{DD}/2$. With (3) and (4) the necessary capacities can be calculated by (5).

$$C_{SH} = \frac{\beta\left(V_{DD} - V_{TH}\right)^2 t_{R,F}}{3V_{DD}} \tag{5}$$

The average current consumption in the level-shifter is determined by the voltage variation of the capacities and the switching frequency f_{SW}. Equation (6) describes this interrelation.

$$I = 2C_{SH}\Delta V_{CSH} f_{SW} \tag{6}$$

In the realized version of a high-voltage switching output stage with dynamic charge pump level-shifter principle the capacities value was determined to 1 pF. The averaging current consumption is approximately 700 nA at a switching frequency of 70 kHz. In Fig. 10 the measured output switching signals are displayed. They indicate a good signal transfer accuracy caused by the reached balance of the delay time between high-side and low-side.

The results of the comparing of the static level-shifter and the dynamic charge pump level-shifter are listed in Table II. The numerical characteristic values of the dynamic level-shifter are expressed relating to its static counterpart. The only disadvantage of the dynamic level-shifter is the not included generation of high-voltage power supply for the high-voltage PMOS driver ($V_{DDH} - V_{DD}$). This disadvantage loses its attached importance for array applications. For that application the second high-voltage rail could be externally provided. As the result the dynamic charge pump level-shifter is consequently the appropriate circuitry for applications like MEMS based switching arrays in wavelength-division multiplexing networks.

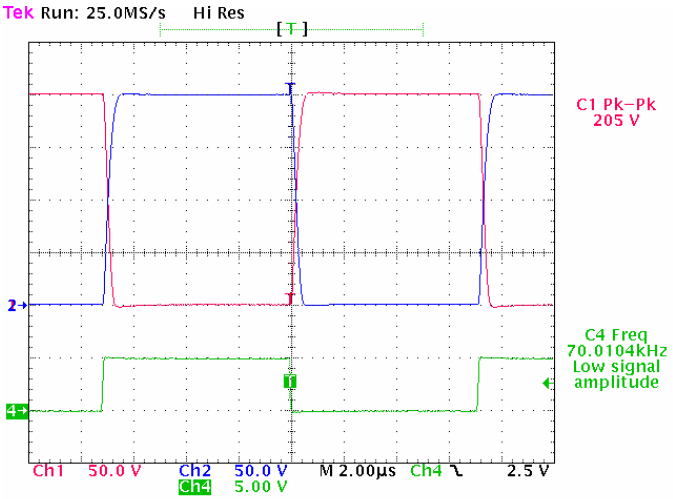

Fig. 10. Measured output signals on the switching output stage included dynamic level-shifter circuitry with charge pump, Ch4: input signal with 70 kHz switching frequency, Ch1: inverted output signal, Ch2: non-inverted output signal

TABLE II
COMPARING OF THE STATIC LEVEL-SHIFTER AND THE DYNAMIC CHARGE PUMP LEVEL-SHIFTER

Property	Static level-shifter	Dynamic charge pump level-shifter
Included generation of the second high-voltage power supply	yes	no
Chip area consumption	100%	12.1%
Current consumption	100%	< 1%
Propagation delay time	100%	13.3%

V. CONCLUSION

The presented dynamic charge pump level-shifter works in a integrated high-voltage class D PWM amplifier designed by alpha microelectronics gmbh. The high-voltage amplifier is separated in two ICs. The multi-channel high-voltage switching output IC is fabricated in a dielectric isolated high-voltage technology. The PWM controller is fabricated in a digital technology and uses the bipolar pulse-width-operation mode described in [1]. The high-voltage IC includes 96 high-voltage output stages and has a chip area of 6.0 mm x 6.5 mm. Every of the 96 output stages generates an inverted and a non inverted high-voltage pulse width modulated output signal, delivered to 192 outputs.

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