Modeling the Leakage Current of Dielectric Isolation Structures in a High-Voltage Semiconductor Technology

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***Abstract*— System-in-package integration becomes more and more important in the growing market of micromechanical sensors and actuators. The most important group of actuators are those based on the electrostatic working principle. Because of the high voltages used to drive these actuators, new methods of isolation need to be introduced. In this paper we will characterize and model the electrical behavior of such an isolation technology. A simple device model to regard parasitic effects of this isolation during the process of circuit design will be introduced.**

I. Introduction

While the minimization of sensors and actuators produced in a MEMS technology has made great progress, this development is of little avail as long as the electronic circuits required to control these micromechanic systems are not integrated within or as close as possible to the system itself. System-on-chip or system-in-package integration are the key technologies to solve this problem.

A nice example for such a system is the Hadamard Transform Spectrometer developed as one project of the collaborative research center "Arrays of micromechanical sensors and actuators" at the Chemnitz University of Technology. The micromechanical part of the system is formed out of an SOI-wafer by several etching steps. The spectrometer utilizes a row of micro-mirrors to implement the Hadamard transformation as described in [1]. The array consists of 48 electrostatic driven torsion-mirrors with an overall length of 7 mm. The surface of the mirrors is coated with a thin layer of aluminum.

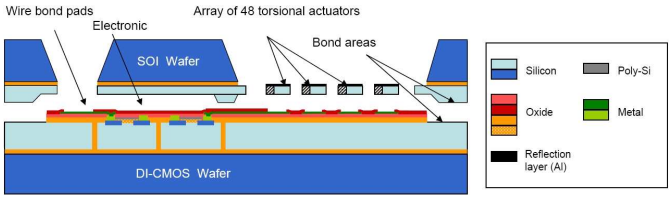

Fig. 1. Schematic cross-section of the wafer compound immediately before the bonding process. [2]

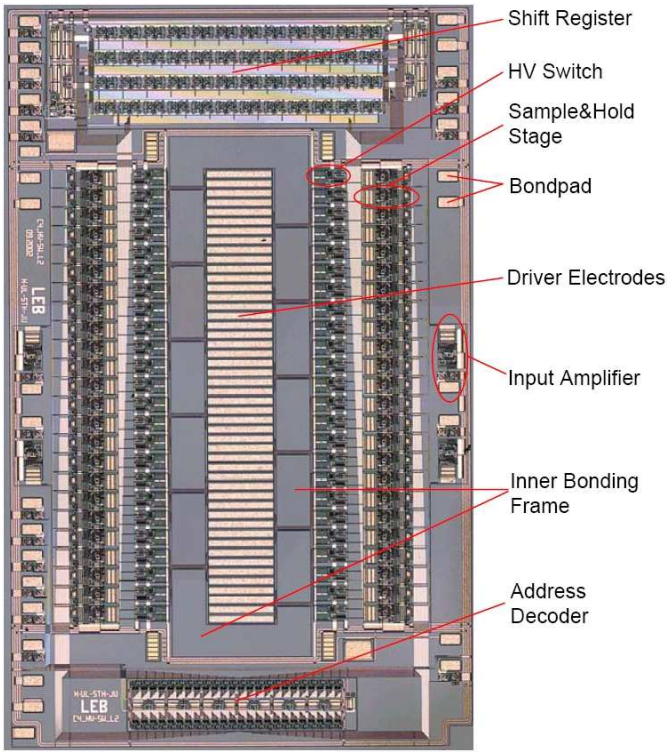

Fig. 2. Photography of the Hadamard Transform Spectrometer without the micromechanical mirror array. [3]

The spectrometer is designed as system-in-package. The micromechanical wafer is combined with the electronics wafer by a low temperature bonding process. Fig. 1 shows a schematic drawing of the wafer compound immediately before the bonding process. The electronics wafer contains the backplate electrodes of the actuators along with the low voltage circuitry

for analog and digital signal processing and the high voltage driver circuits [3].

As shown in Fig. 2, the layout of the circuit is dominated by the backplate electrodes and the bond frame needed to combine the two wafers. In connection with the high voltage driver electronics, certain requirements for the underlying technology can be formulated. The isolation structures used in this technology must provide a good isolation at high voltages while consuming a minimal amount of physical space.

II. Dielectric Isolation Structures

Classic bipolar or CMOS technologies widely rely on junction isolation. While this isolation method can also be applied to high voltage circuits, there are significant drawbacks. The leakage current associated with this isolation is not zero and has very high temperature dependence. Additionally, the junction works as a voltage dependent capacity, limiting the maximum frequency of operation. The greatest downside in using junction isolation in high voltage circuits is the occupied physical space. The depletion region of the reverse biased junction becomes wider as the supply voltage increases, thus limiting the possible degree of integration.

Using a dielectric isolation technology to electrically separate single devices helps to overcome those drawbacks. This type of isolation provides very low leakage current and minimal space consumption. An overview of different dielectric isolation technologies can be found in [4].

In cooperation with the X-FAB Semiconductor Foundries, the electrical behavior of such an isolation technology was characterized. The examined isolation structures were samples made in a 1 µm fully dielectric isolated smart power process. The process features high voltage DMOS transistors along with CMOS transistors with different voltage levels and bipolar devices.

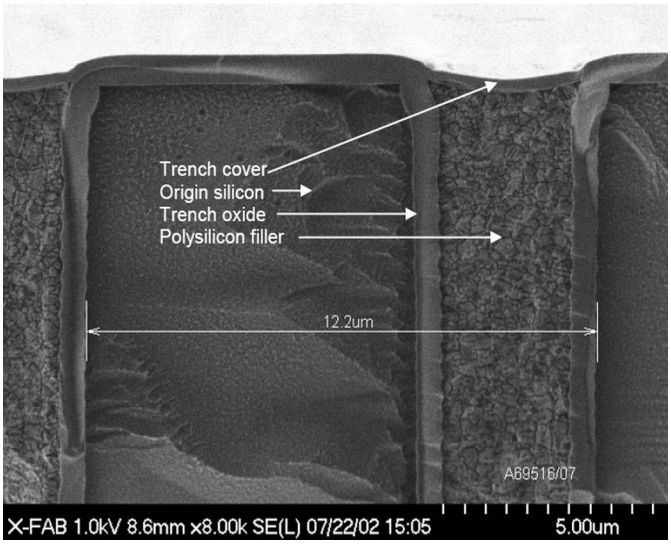

Fig. 3. Cross-section of the finished trench isolation structure with cover oxide. The vertical isolation layer formed by the buried oxide is not shown. [5]

Fig. 3 shows a cross-section of the isolation structure used within this process. The vertical isolation is provided by a thick buried oxide. Lateral isolation is realized by a trench with very high aspect ratio. The silicon at the trench sidewalls is highly doped and functions as low resistance contact area to a buried N+ layer. The sidewall oxide ensures the insulating capability. Finally, a polysilicon refill provides the mechanical stability of the structure. The maximum operating voltage for the isolation structures is specified with 300V for a single trench. By using parallel trenches, the maximum voltage can be raised up to 700V for a triple trench.

III. Electrical Characteristics

During our research, the dependence of the leakage current of these isolation structures on the applied voltage and device temperature was measured. The determined electrical behavior was quite complex. The leakage current shows a strong dependence on the history of electrical stress the isolation structure was exposed to. An unstressed trench initially shows a leakage current which will immediately decrease while stressing the structure with constant voltage. We will refer to this effect as electric formation of the trench.

A. Electric Formation

The typical leakage current characteristic of an unstressed trench is shown in Fig. 4. As mentioned, the leakage current initially decreases rapidly with the rate of decrease being clearly voltage dependent. Further investigations also revealed a dependence of this formation effect on the polarity of the applied voltage. A trench already stressed behaves like an unstressed trench if the polarity of the applied voltage is reversed. In addition, the structure undergoes a new formation cycle if stressed with a higher voltage than before. Even after very long durations of electrical stress, the trench leakage current did not saturate at a distinct level. Also, the effect can not be reversed.

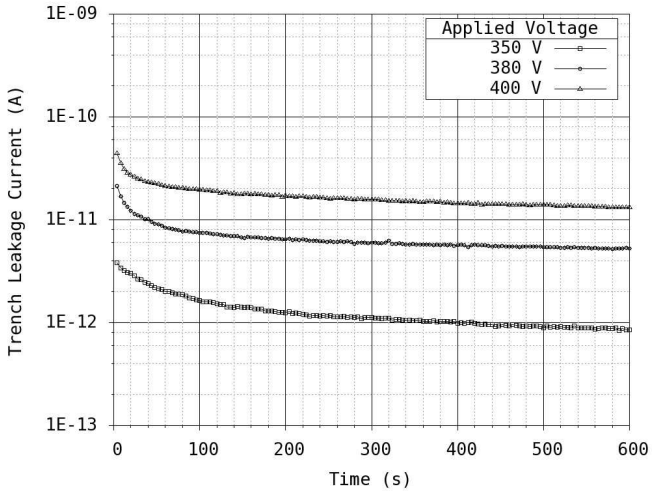

Fig. 4. Measured leakage current characteristic of the trench while being stressed with a constant voltage. [6]

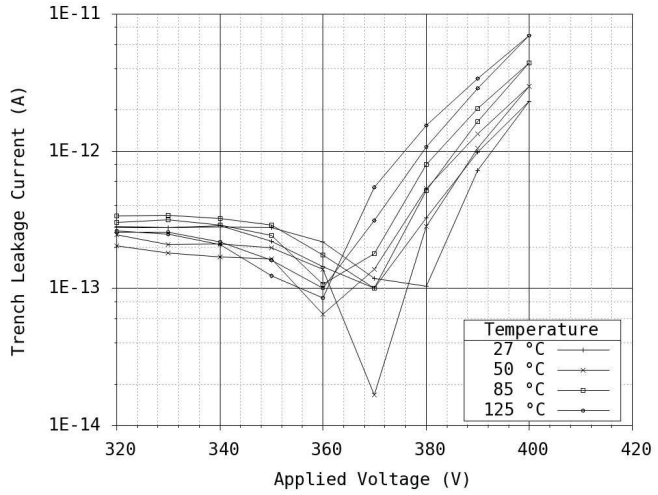

Fig. 5. Measured dependence of the trench leakage current on device temperature and applied voltage. [6]

The underlying physical principle leading to this behavior seems to be the charging and discharging of traps in the sidewall oxide of the trench. As described, the sidewall isolation is formed by oxidation of highly doped silicon. Such oxides are known to contain a high concentration of structural defects [7], [8]. Depending on the nature of the defects, they can act as trapping centers for positive or negative carriers traveling through the insulating layer.

The creation of a device model was very much complicated by this effect. A special model for unstressed isolation structures had to be created. Because of the rapid formation process, measurement of the leakage characteristic of such an unstressed trench was not possible. The according worst case model had to be derived from the characteristics shown in Fig. 4.

B. Leakage Current Characteristic

An example for the typical voltage dependence of the trench leakage current at different temperatures can be found in Fig. 5. Because of the ongoing formation effect during measurement which can be seen in the hysteresis of the curves, different structures had to be used for each device temperature. All devices were exposed to the same electric stressing before each measurement.

The leakage current shows a distinct, nearly exponential dependency on the applied voltage. The influence of the device temperature on the leakage current is not very strong but still had to be taken into account for our model.

IV. Modeling and Simulation Results

With simulation being a key part in today's process of integrated circuit design, the existence of proper device models becomes crucial. This need also applies to parasitic circuit elements like isolation structures. For dielectric isolation technologies like the one investigated, such models don't exist yet.

A. Generic DC Model

As already described, the isolation structures are composed of two layers of silicon dioxide with a layer of low doped polysilicon embedded between. With the specific conductivity of polysilicon being several orders of magnitude higher than that of the oxide, the main voltage drop occurs above the two layers of oxide. With a negligible voltage drop above the polysilicon, the influence of this layer on the static leakage current characteristic could be neglected. Therefore, the leakage current was described by modeling the carrier transport through a single dielectric layer surrounded by highly doped n-type silicon.

Looking at carrier transport in insulating layers, different physical processes have to be taken into account. A short overview on different mechanisms of carrier transport is given by Sze [9]. In our case, tunneling of electrons through the energy barrier formed by the oxide was determined as the main carrier transport phenomenon.

$$J = A \cdot E^2 \cdot \exp\left(\frac{B}{E}\right) \tag{1}$$

Under large applied bias, the density of the tunneling current can be described by (1), with E being the average electric field in the oxide layer and the constants A and B depending on the energy barrier height φ_B at the Si-SiO_2-interface and the effective electron mass m^*_{Ox} in the dielectric as shown in (2) and (3) [10]. q is the electronic charge, m_e is the electron rest mass and h is Planck's constant.

$$A = \frac{q^3 m_e}{8\pi h m^*_{Ox} \varphi_B} \tag{2}$$

$$B = -\frac{8\pi\sqrt{2m^*_{Ox}\varphi_B^3}}{3qh} \tag{3}$$

This equation is only valid for a triangular barrier. As mentioned, the oxide layer contains a large number of structural defects. These trapping centers can be neutral, negative or positive charged, causing a deformation of the energy barrier. As shown in Fig. 6, this deformation changes the tunneling

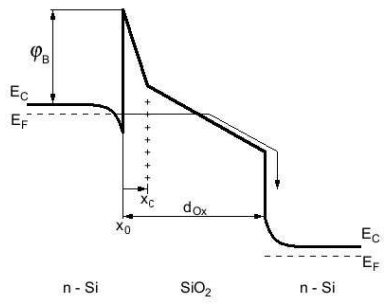

Fig. 6. Deformation of the energy barrier under influence of positive charge. The charge distribution has been simplified as a sheet charge. [6]

distance for the electrons. To get a universal equation for the tunneling current, one would have to resolve the derivation of (1) for an arbitrary shape of the barrier.

Because of the complexity of this derivation, we approximated the influence of the varying tunneling distance by introducing an effective barrier height $\varphi_{B,eff}$ into (2) and (3). By simplifying the unknown distribution of oxide charges with an charge sheet close to Si-SiO_2-interface, this effective barrier height can be expressed by (4). Q' represents the equivalent density of charges. The distance of the charge centroid from the interface is expressed by x_c.

$$\varphi_{B,eff} = \varphi_B - \frac{q \cdot x_c \cdot Q'}{\epsilon_{SiO_2}} \tag{4}$$

The tunneling of electrons is usually assumed to be independent of the device temperature. For the tunneling probability of an electron itself, this assumption is valid. Nevertheless, with the energetic distribution of electrons in the semiconductor being temperature dependent, the temperature dependence of the tunneling current can not be neglected. As shown by Suñé, this temperature dependency can be explained by electrons occupying higher subbands in the accumulated silicon close to the interface [11]. Therefore, the influence of device temperature on the tunneling current was also introduced into our model as a lowering of the effective barrier height. The temperature dependent barrier lowering $\Delta\varphi_{B,eff}$ was approximated by (5) with TK_{φ_B} being the temperature coefficient.

$$\Delta\varphi_{B,eff}(T) = -TK_{\varphi_B} \cdot \left(\exp\left(\frac{T}{T_{nom}} - 1\right) - 1\right) \tag{5}$$

Fig. 7 exemplarily shows the simulation results for the created SPICE model. The model parameters for the barrier height at the Si-SiO_2-interface $\varphi_B = 3.12\,\text{eV}$ and the effective electron mass in silicon dioxde $m^*_{Ox} = 0.5 \cdot m_e$ are standard values taken from [9]. The fitting was done via the equivalent

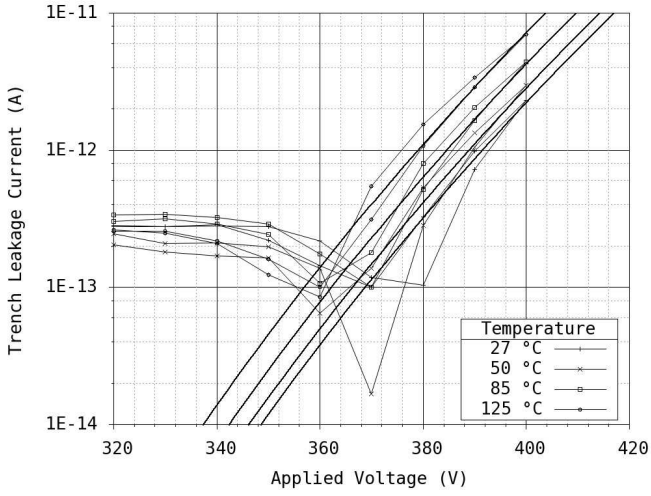

Fig. 7. Simulation results of the static DC-model. [6]

density of charges Q' and an additional temperature coefficient. The centroid of the charge distribution was assumed to be in a distance of 10 nm from the Si-SiO_2-interface. As visible, temperature and voltage dependence of the trench current can be very well recreated.

B. Worst Case Model

The model presented so far is only valid for a trench exposed to a specific amount of electric stress. The model can therefore only be used to simulate the typical mean behavior of the isolation structures. The higher leakage current of an unstressed trench has to be regarded in terms of a worst case model.

As said before, the characteristic of an unstressed trench can not be measured directly. Instead, the according SPICE model has to be derived by modeling the process of electric formation itself. By following our assumption of a distribution of positive charged traps close to the Si-SiO_2-interface, a simple model for the filling process of these traps was created. Only the neutralization of positive charged traps was considered in this model. The temperature dependence of the process was not regarded.

In addition to the single positive charged trap distribution Q' considered for the model of the stressed trench, a time-dependent density of charges Q'_t was introduced. During the tunneling process, the electrons are passing an area with a high concentration of traps. Every electron has certain probability to neutralize one of these positive charged traps. The time-dependent concentration of traps $Q'_t(t)$ can therefore be described by (6). $J(t)$ is the time-dependent tunneling current density, α' expresses the probability of a trap neutralization process by a single electron.

$$\frac{dQ'_t(t)}{dt} = -\alpha' \cdot Q'_t(t) \cdot \frac{J(t)}{q} \tag{6}$$

By taking (1) - (4) to express the tunneling current density, the differential equation can not be solved analytically. Instead, we approximated the current density by a simple exponential function depending on the applied voltage and the density of traps. This assumption is valid for a trench stressed with a constant voltage, as in our measurements (see Fig. 4). With the boundary conditions $Q'_t(t=0) = Q'_{t,0}$ and $Q'_t(t=\infty) = 0$, the time-dependent part of the trap concentration can be approximated by (7). The fitting parameters α and β were extracted from the measured curves. The two parameters showed only minor deviation for all analyzed isolation structures and applied voltages.

$$Q'_t(t) = Q'_{t,0}\left(1 - \sqrt{1 - \exp\left(-\alpha \cdot t \cdot \exp\left(\beta \cdot V\right)\right)}\right) \tag{7}$$

With this approximation, the static DC-model was enhanced. Equation (4) was extended with an additional barrier lowering caused by the time-dependent part of the trap concentration. As the degree of electric formation rises with the applied voltage, the two charge densities Q' and $Q'_{t,0}$ vary. An additional exponential voltage dependence had to be applied

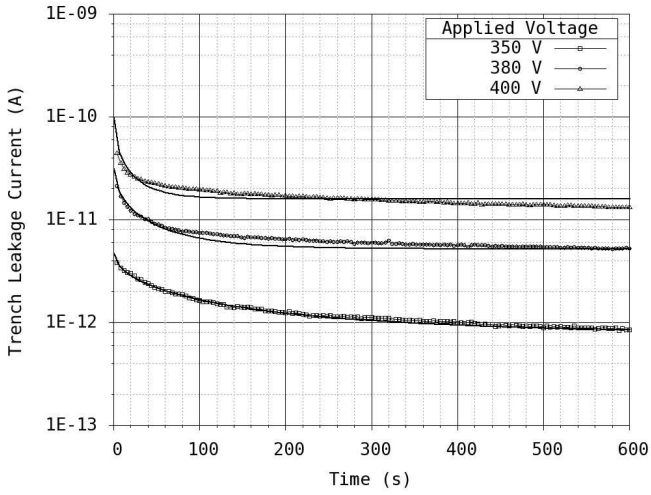

Fig. 8. Simulation results for the time-dependent leakage current. [6]

on both parameters to fit the measured curves. Equation (8) shows the time-dependent effective barrier height.

$$\varphi_{B,eff}(t) = \varphi_B - \frac{qx_cQ' \exp(\gamma V)}{\epsilon_{SiO_2}} - \frac{qx_cQ'_{t,0} \exp(\delta V)}{\epsilon_{SiO_2}} \quad (8)$$

By combining (7) and (8) with the static DC-model, the formation process could be simulated. The simulation results for the new time-dependent model can be seen in Fig. 8. Due to the approximations made, the model is only valid for low applied voltages and a short loading duration. For voltages within the specified operating conditions, the model provides accurate results. With the parameters extracted, the final worst case model for the isolation structures was created by evaluation the time-dependent model at $t = 0$.

V. Conclusion

A simple device model to regard parasitic leakage currents in an fully dielectric isolated high voltage semiconductor technology was developed. The model can accurately recreate the temperature and voltage dependence of the static leakage current. A second model reflects the time dependent behavior of the isolation, enabling the creation of a worst case model. Both models can be easily implemented in any SPICE compatible circuit simulator.

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