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Electrical Analysis of Integrated Field Effect Transistors as Electromechanical Transducer for Stress

Introduction

The growing need to develop very small sized integrated sensors in the MEMS/NEMS field is a strong motivation to research new transducers, which consume less power and less on-chip area resulting in less cost. Field Effect Transistor (FET) can meet these requirements. Based on the property of piezoresistive effect in silicon, MOSFETS can be used as mechanical strain transducers, in which mechanical stress influences the mobility of charge carriers in the channel of a FET and hence its resistance In this work a pressure sensor, consisting of a silicon membrane and transistors is designed and manufactured using 1.0 µm-XC10 technology. The transducers for mechanical stress are placed on the edges with the maximum stress. Furthermore, the position is optimized by using FEM simulations (Ansys). Transistors are manufactured in different channel doping, lengths, widths, and alignments of the channel current to the direction of the mechanical stress to be investigated as well as connecting transistors in wheatstone-like quarter and half bridges to generate a read out voltage.

Principle of Operation: Piezoresistive Effect in Silicon

$$I_D \propto \mu \quad \Rightarrow \quad I_D \propto \mu_0\left(1-\pi_\parallel\sigma_\parallel-\pi_\perp\sigma_\perp\right)$$

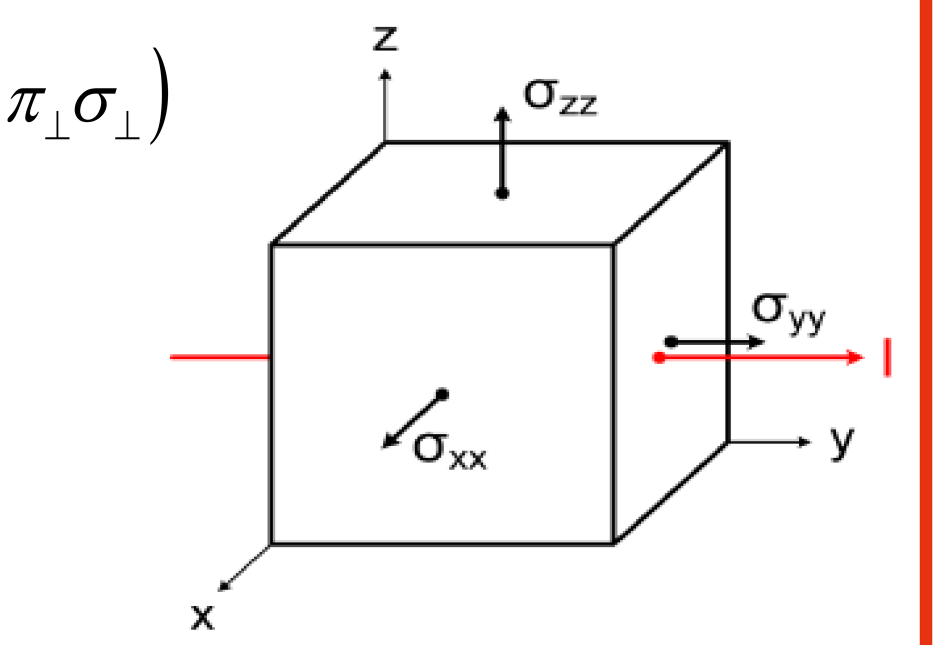
I_D : Drain current

μ_0 : Intrinsic mobility of charge carriers

$\pi_\parallel, \pi_\perp$: Parallel and vertical channel piezoresistive coefficient

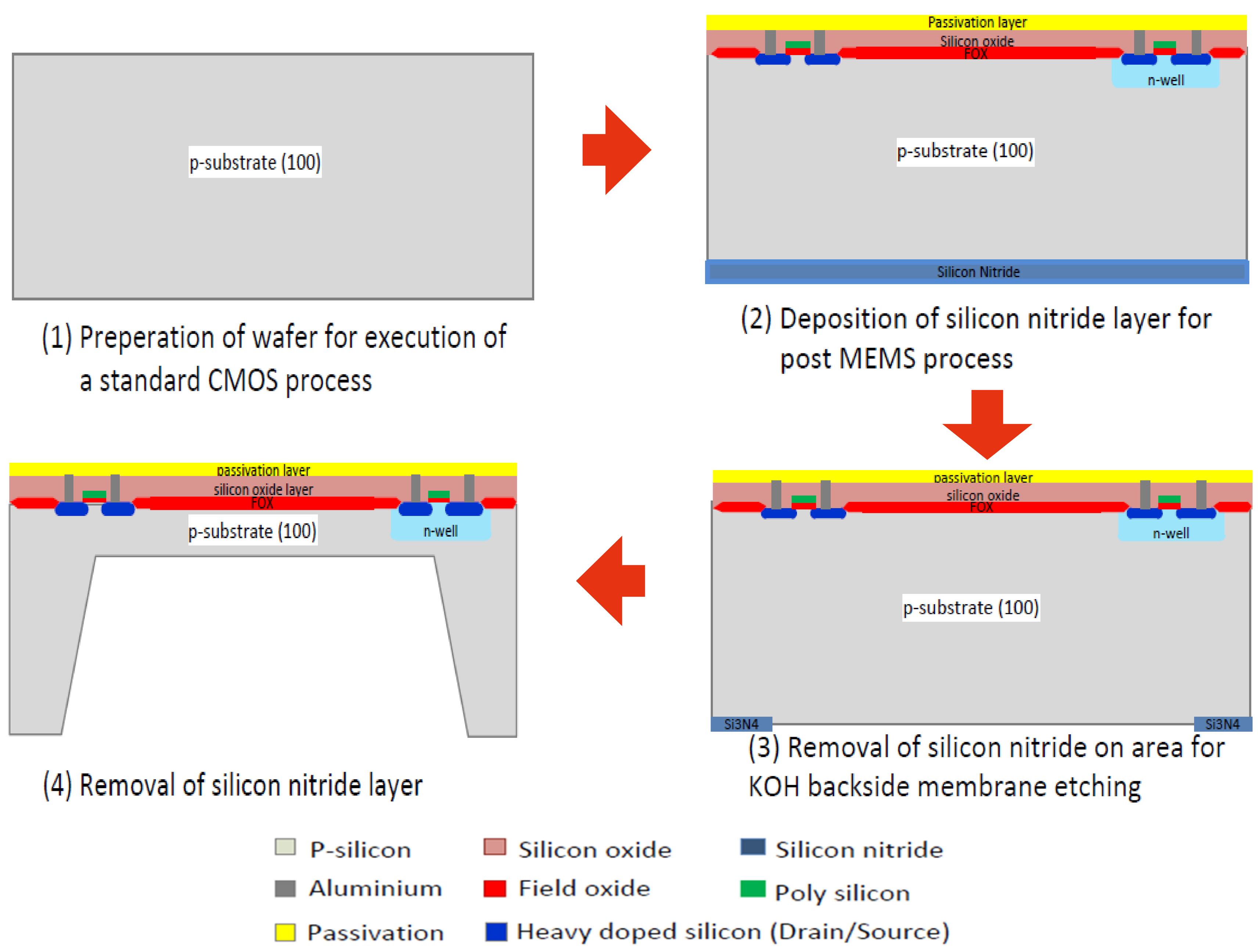
$\sigma_\parallel = \sigma_{yy}$: Parallel stress in the channel

$\sigma_\perp = \sigma_{xx}$: Vertical stress in the channel



An infinitesimal cubic element in Silicon membrane with normal stress components shown on its faces. The red line represents the current flow in the transistor channel

Manufacture in Technology XC10 by XFAB



(1) Preperation of wafer for execution of a standard CMOS process

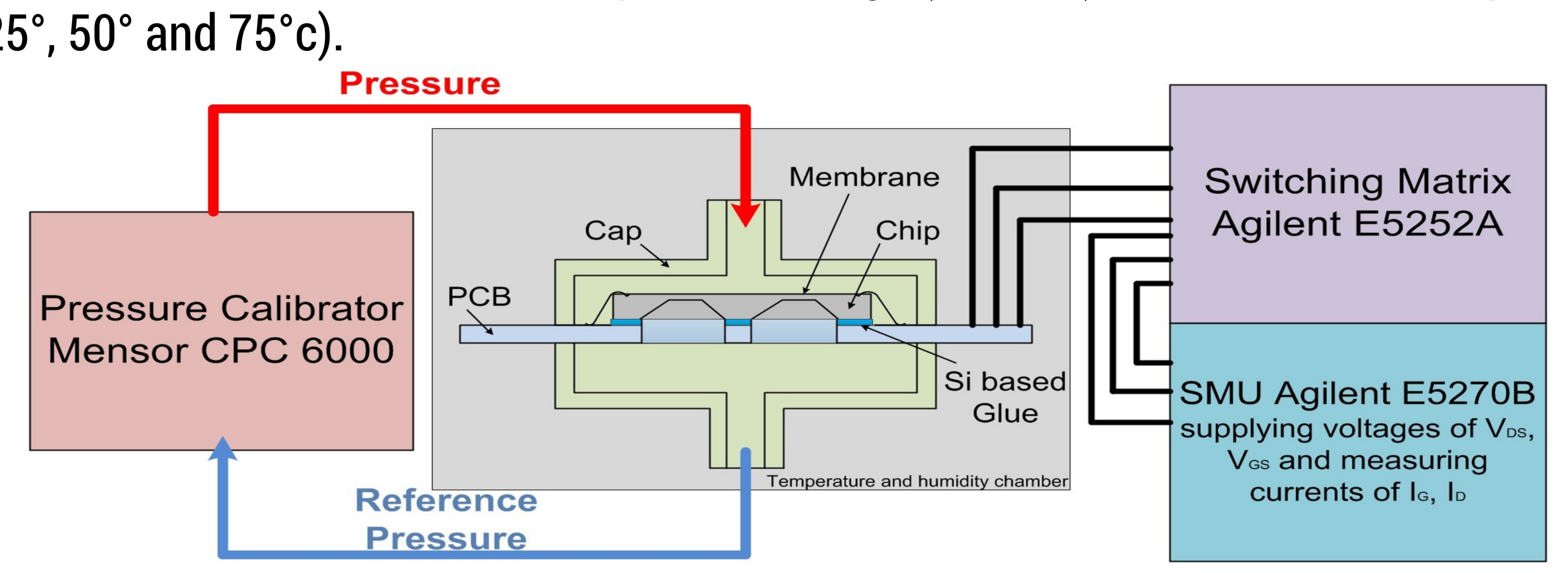
(2) Deposition of silicon nitride layer for post MEMS process

(3) Removal of silicon nitride on area for KOH backside membrane etching

(4) Removal of silicon nitride layer

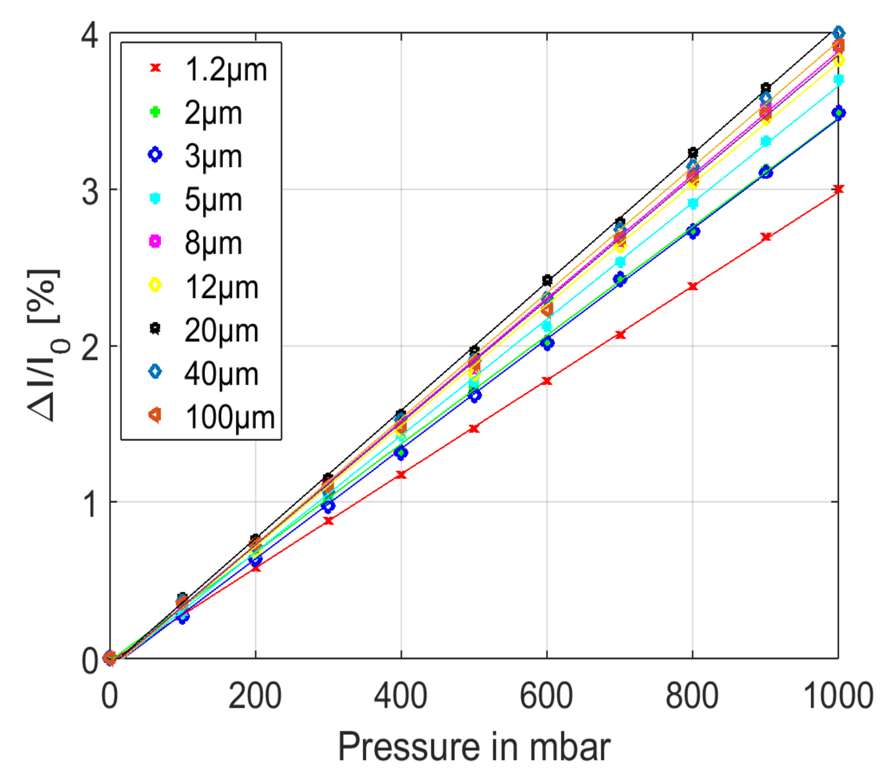
Experiment Setup for Chips Characterization

Individual Transistors are tested in pressure range (0 -1 bar) under different temperatures (25°, 50° and 75°c).

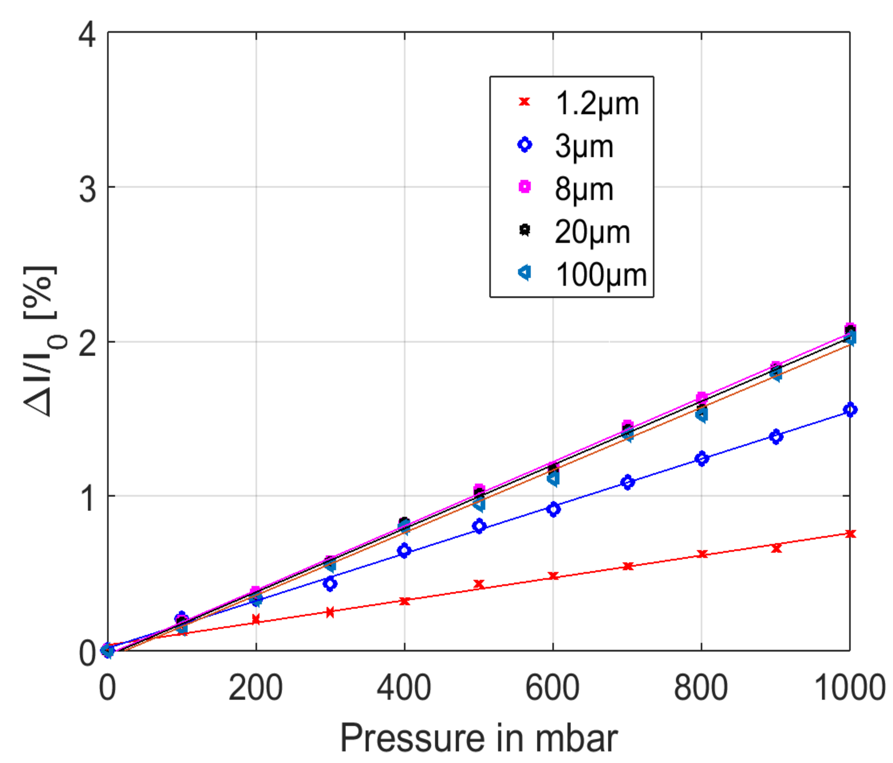


Experiment setup for variable applied pressure and temperature

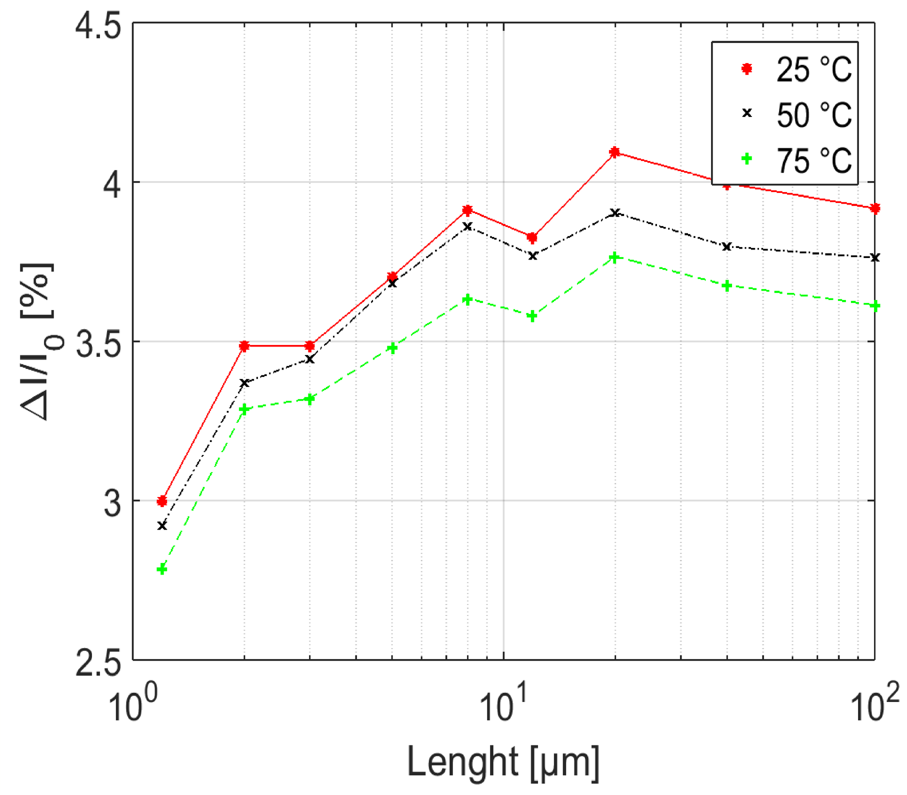
Transducer Sensitivity for different Channel Lengths under different Temperatures



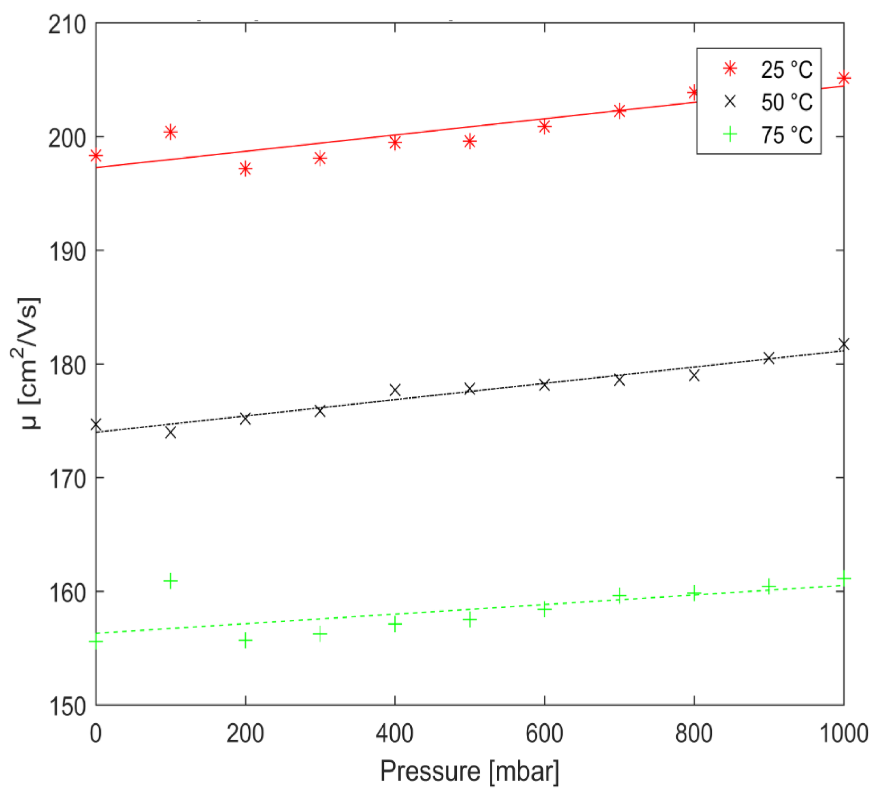
Normalized current change of p-MOSFETs with different channel lengths and constant channel width(W=8 µm) at T=25°C



Normalized current change of n-MOSFETs with different channel lengths and constant channel width(W=8 µm) at T=25°C



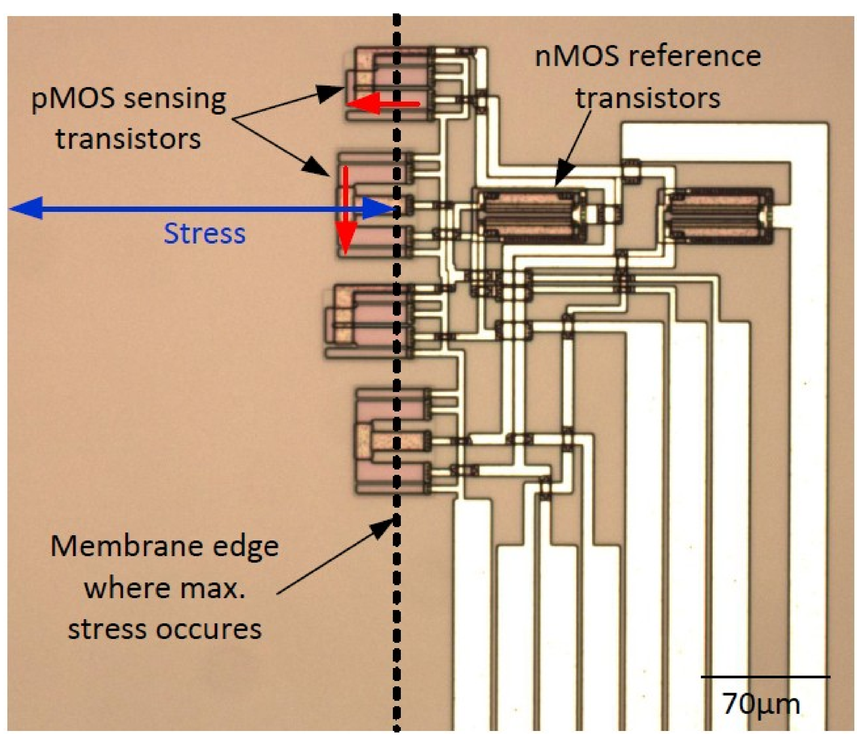
Normalized current change with respect to channel length for different Temperatures of a group of p-MOSFETs



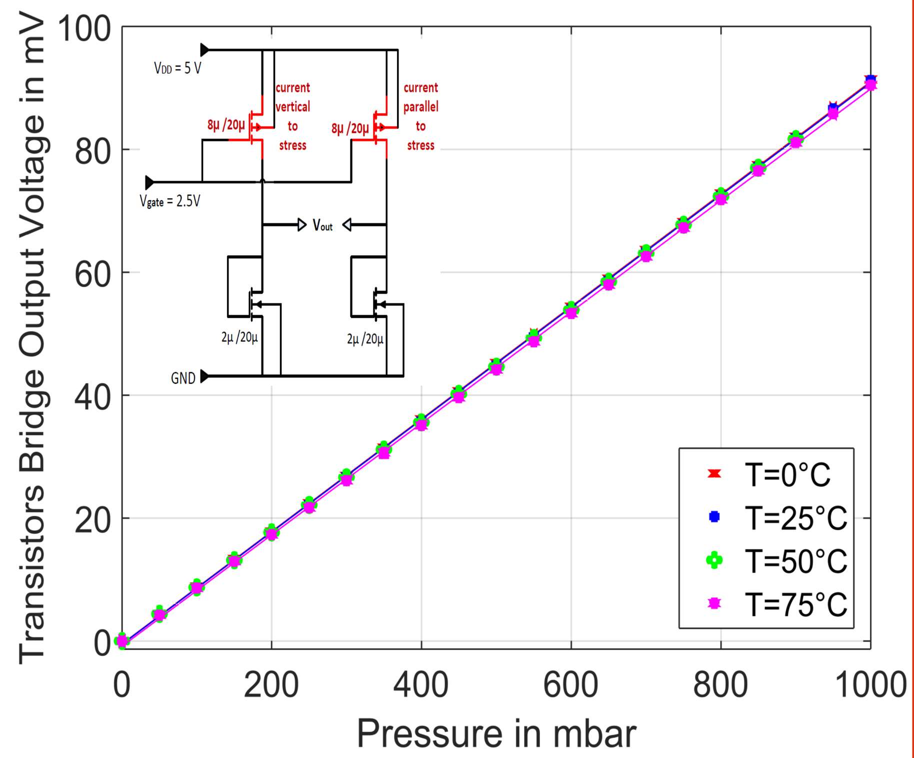
Change in mobility of charge carriers in the channel of a p-MOSFET (W/L=8/20) with pressure for different Temperatures

Compensation of Temperature Influence

Connecting the transistors in a half bridge-like circuit. The p-MOSFETs are positioned in different directions to stress. The calculated TC of the bridge is -130 ppm/K.



Microscopic image of a half bridge-like of transistors placed on the edges of an 1x1mm² membrane at max. stress. Red lines represent I_D



Pressure and temperature dependency of a bridge-like circuit of transistors

Summary & Acknowledgement

- Very high Temperature Coefficient of individual transistors. TC of bridge-like circuit of transistors is very low compared to piezoresistors bridge.
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