Alternative level shifting devices for 900V gate drivers

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Abstract

With increasing operating voltages the size of high voltage transistors used as level shifters increases tremendously. For 900V applications the area consumption would get cost critical. Alternative level shifting concepts make use of capacitive, inductive or optical coupling. The appropriate integrated high voltage devices were developed and the functionality verified. 900V capacitors as well as inductors with 900V isolation capability can be built with existing process layers. For integrated light emitting diodes a III-V material stack based on GaP for epitaxial growth on standard CMOS wafers and Ga(NAsP) as quantum well material system was used. Functional devices as well as functional signal transfer behaviour could be demonstrated for all approaches with significantly reduced area consumption.

Keywords: integrated high voltage devices, level shifter, trench isolated SOI

INTRODUCTION

In future, social and legislative demands for higher power efficiency will strongly affect the design of three phase drives e.g. for industrial motor applications. This will increase the need for regulated motor drive modules and appropriate high voltage gate driver ICs with high side capability, robustness against negative voltage output spikes and certain logic functionality. For 400V three phase applications usually 1200V IGBTs and freewheeling diodes are used. The 400VAC from the three phase supply result in a dc link voltage of about 560V, with 10% tolerance the maximum dc link voltage is 620V, with an additional safety margin at least 900V operating voltage are required for the gate driver ICs. A trench isolated SOI process with appropriate operating conditions was developed for this application.

An example for a half bridge gate driver IC is shown in figure 1. The complete half bridge driver consists of several blocks. The input is formed by a first level shifter which features an independent logic supply VDD (typical 3V to 5 V). The input signals IH and IL are shifted to the level of VDDLS (typ. 15V). The shifted signal IL is then fed into the low side gate driver (lower part of the schematic) consisting of a push pull driver with a current capability of 250mA. The shifted signal IH is connected to a driver matched to the several possible types of high voltage level shifting devices. On the high side part of the driver (upper part of the schematic) a flip flop senses the signals transmitted from the low side. This flip flop is also matched to the different types of shifting devices. Both high and low side part of the half bridge driver feature an under voltage lock out circuit (UVLO) which turns off the external IGBT at low supply voltage (typ. < 10V). Especially the high side UVLO and flip flop have very low current consumption (typ. 100µA) to lower the load for the external bootstrapped supply. The low side part also features a fast opamp (GBW 10MHz) for current sensing across the external source shunt resistor RS. A window comparator is also integrated to detect bidirectional overcurrent faults. Both circuits are not shown in the schematic for clarity.

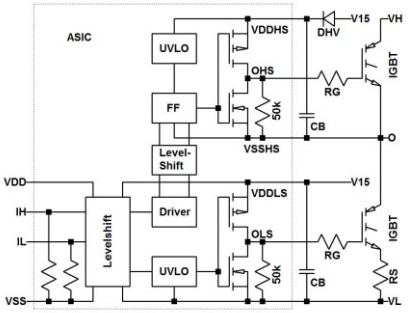

Figure 1: Gate drive schematic with level shifter

Normally, high voltage transistors are used as level shifters to transfer signals between low side logic and high side driver. In total - with three high side channels, two

transistors for a bi-directional signal transfer and supplemental two transistors in case of prevailing differential level shifting – up to 12 level shifters are required. Higher operating voltage requirements imply a significant increase in the required footprint of the high voltage devices, see Table 1. Several square millimetres of chip area just for the 6-12 level shifters would be a significant cost factor.

Breakdown voltage [V]	450	620	730	1050
Device area [mm2]	0.03	0.05	0.14	0.53

Table 1: Device area for quasi-vertical DMOS transistors with different breakdown voltages.

But alternative concepts like capacitive, inductive or optical coupling need corresponding high voltage capacitors, inductors or integrated light sources and detectors. These devices were developed, investigated and will be compared to standard high voltage transistors with regards to area needs and signal transfer ratios.

900V PROCESS EXTENSION

A trench isolated SOI process with 900V operating voltage [1], [2] was used as baseline process. Isolation requirements are fulfilled by a thick buried oxide and double trench isolation. SOI thickness and doping allow the construction of robust quasi-vertical DMOS transistors as standard level shifter. The three layer metallization uses normal Inter Metal Dielectric (IMD) between metal 1 and metal 2 but a thick IMD oxide between metal 2 and metal 3, the passivation is reinforced by a polyimide layer.
With this process setup quasi-vertical DMOS devices were developed with breakdown voltages above 1000V, Table 1. With a size of about 0.5mm² they act as a reference in area consumption of the different level shifting devices.

CAPACITIVE COUPLING

Device Description

For capacitive coupling several capacitor topologies were examined for their usage as 900V capacitors:

- Sandwich capacitors, consisting of a vertical stack of polysilicon, metal 2 and metal 3 plates where metal 3 and polysilicon capacitor plates are connected. Isolation between capacitor plates is thick Inter Metal Dielectric (IMD) oxide and Inter Layer Dielectric (ILD) + IMD respectively
- simple planar metal plate capacitors: e.g. metal 2 – metal 3 capacitors with thick IMD isolation in vertical direction or polysilicon– metal 3 capacitors with an isolation consisting of thick IMD, thin IMD and ILD oxide
- fringe capacitors with vertical capacitor electrodes made by metal 1 plus metal 2 plus metal 3 (no dedicated via metal in this process). Isolation is done by lateral spacing
- trench capacitors with square and meander layouts of the trenches

These devices were compared with regards to voltage capability and capacity.

Results

For the different capacitor structures and current-voltage-characteristics, some examples shown in Figure 2 or breakdown voltages and the capacity were measured as wafer maps.

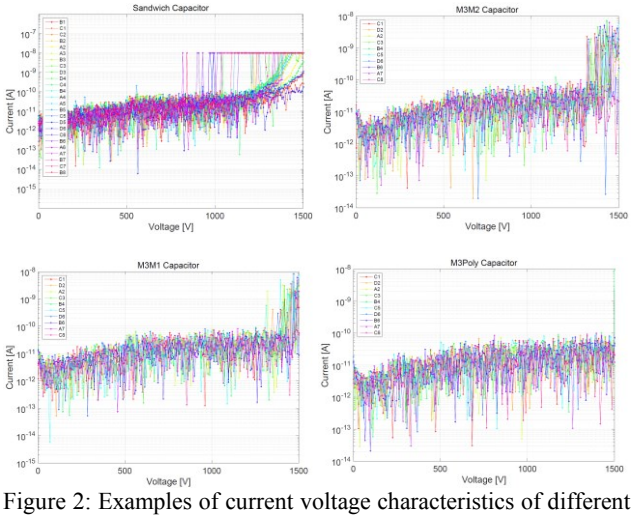

Figure 2: Examples of current voltage characteristics of different capacitor structures

Capacity and operating voltage results are summarized in Table 2. The "maximum operating voltage" in Table 2 was defined as the lower value of the onsets of a leakage current and the occurrence of current spikes respectively. E.g. for metal 3 / metal 1 capacitor the leakage current increases at 1300V while for the sandwich capacitor already at about 800V first current spikes were detected.

Capacitor type	Capacitance per area	Maximum operating voltage
fringe cap, 5µm spacing	3.4 aF/µm²	600V
trench cap, square layout	38 aF/µm²	650V [2]
trench, meander layout	36 aF/µm²	650V [2]
Sandwich capacitor	28 aF/µm²	750V
Metal plate M3-M2	15 aF/µm²	1200V
Metal plate M3-M1	11 aF/µm²	1300V
Metal plate M3-polysilicon	9 aF/µm²	>1500V

Table 2: comparison of different capacitor structures

Discussion

All measured capacitor structures achieve operating voltages of 600V and above, nevertheless only the metal plate capacitors can be operated up to the required 900V without leakage or single spike arching issues. Reasonable capacitance values per area together with operating voltages above 1200V were found for the metal 3 – metal 2 capacitor. Additional safety margin at the expense of slightly lower capacitance can be achieved with the metal 3 – metal 1 capacitor.
The functionality of the capacitive coupling concept was proven by means of a preliminary demonstrator IC. An operating capacitive coupling level shifter was demonstrated using metal 3 – metal 1 capacitors even though issues with parasitic capacities within the trench isolated SOI baseline process were witnessed.
The capacitance needed for proper signal transmission is a trade-off between driver strength, input resistance of the flip flop, propagation delay of the flip flop and parasitics. Especially long parallel signal paths like bond wires introduce large parasitic capacitors that attenuate the flip flops input signal by shunting. Also the underlying tubs, trenches and handle wafer form parasitic capacitors that attenuate the transmitted signal and load the driver. The input resistance of the flip flop in combination with the shifting capacitors forms a high pass with a decaying exponential voltage waveform at the flip flops input. So the flip flop has to change its state before the signal has decayed too much for being sensed. Also the common mode failure currents through the capacitors produce a voltage signal at the flip flops input during commutation of the external IGBTs. The amplitude of these failures signals must be smaller than the trigger level to avoid a change in the flip-flop state. This trade-off has led to several capacitance values for different application scenarios. In a split die approach with approximately three millimeters of bond length between the dice a capacitance of 1.5pF has been proven. This capacitance was reduced to 1pF in a single die approach though it is possible to further reduce the capacitance to approximately 0.3pF by increasing the input resistance of the flip-flop.

INDUCTIVE COUPLING

Device Description

Since lateral coils were found to have a very large process variation the focus was on planar inductors. First 2D simulation showed a trade-off between the coupling factor versus the number of windings, see Figure 3. Additionally, the coil resistance as well as the coil area also increase with the number of windings. For coil to coil inductive coupling, 5 different octagonal coreless transformers ("1" to "5") with 33 windings (or a coupling coefficient of 0.95) were designed and processed: displacement, rotation and winding direction were varied to investigate different coupling paths inside the IC.

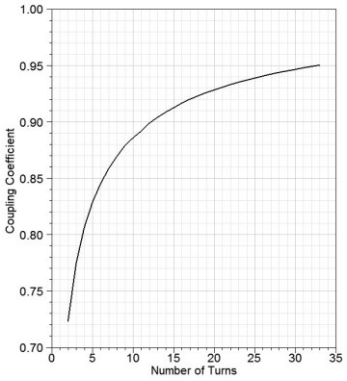

Figure 3: Simulated coupling coefficient versus the number of windings

Results

The processed coil variants were characterized in terms of resistance and coupling. The resistivity of the different coils was found to be very constant indicating a stable and reproducible design and micrometer scale processing as a prerequisite for further analysis.
The influence of the coil layouts can be seen in Figure 4. The signal transfer ratio can be improved from 0.1 to 0.25 at higher frequencies with an optimized layout.

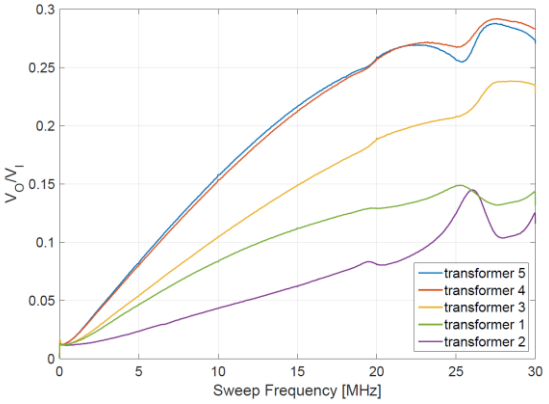

Figure 4: Signal transfer ratio (output voltage Vo / input voltage Vi) versus frequency for different coil coil transformer designs

Different characterization methods have been used to evaluate the coil to coil coupling and to separate effects of parasitic capacitances from the inductive coupling. The result of a sinusoidal signal on the input is shown in Figure 5. For practical use in an application the devices have also been tested with rectangular signals. With higher slew rates (lower rise time) of the input voltage the peak to peak voltage of the output signal increases, Figure 6.
A complete magnetic 3D FEM simulation model had been evaluated and discarded due to the large computational effort at limited precision. Therefore a simplified Spice

model with shorter simulation times was developed. Results of this simulation model are compared to measurement values in Figure 5.

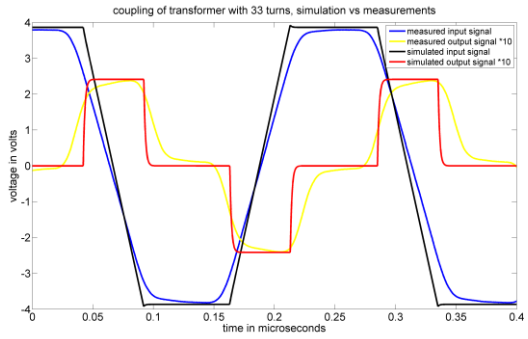

Figure 5: Measured input signal (blue, simulated input signal (black), 10* measured output signal (yellow), 10*simulated output signal

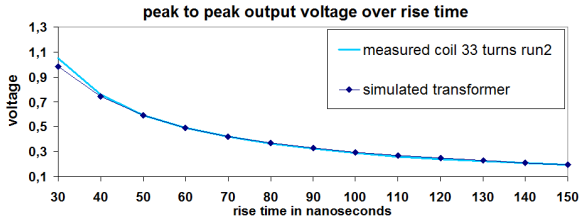

Figure 6: output peak to peak voltage versus input signal rise time

Discussion

The applied slew rates, coil layouts, number and resistances of the coil windings were identified experimentally and by simulation to be the most important parameters affecting the signal transfer ratio (=input to output ratio). Simulations and measurements of signal transfer ratios up to 0.25 (or -12dB) at 20MHz demonstrated the feasibility of integrated inductive signal transfer.

The major benefit of an inductive shifting device is the separation of the inductive signal path and the parasitic capacitances. With a clever arrangement of the coils and their windings it is possible to minimize the parasitic effects. This can be accomplished by a shielding layer between the two coils. So in this shifting approach only one coil is needed for transmitting both the set and reset command in comparison to the DMOS or capacitive shifter approach where two devices are needed to transmit both commands.

A big challenge for the coil driving unit is the relatively short rise time for the input signal. Because of the necessity of having an output voltage amplitude in the range of 0.5 volts to get an adequate signal to noise ratio there is the need of 30ns rise time input signal. This might be the biggest challenge to get a good inductive coupling device.

A good agreement especially in the amplitudes between the simplified Spice model and the measured behaviour was found with a slightly more rounded behaviour in the measurements. The developed and tested Spice model is a good tool for further investigations.

OPTICAL COUPLING

Device Description

For integrated optocoupler light emitting diodes based on a III/V material stack were integrated onto CMOS <100> wafers. The layers were grown in an industrial 300mm cluster tool. The AIXTRON Crius cluster tool consists of two 300mm reactors and a Brooks robot system. The material stack is shown schematically in Figure 7 and consists of an intermediate thin GaP layer, differently doped n-contact layers, waveguide layers with large refractive index, the optically active single quantum well structure, differently doped p-contact layers and a final contact layer. Details on the Ga(NAsP) MOVPE growth are given in [3] and [4].

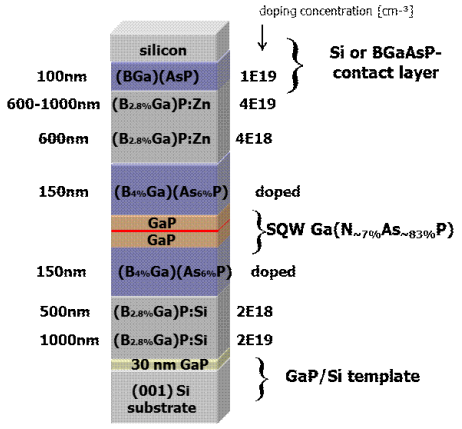

Figure 7: thicknesses, materials and doping levels of the LED stack

The integration of the selective Metal Organic Vapour Phase Epitaxy (MOVPE) was done inside opened Inter Level Dielectric (ILD) islands on 1µm CMOS wafers [5] with single poly and single metal.

Results

The CMOS transistors were checked after the III/V MOVPE process with output characteristics in three different flows, Figure 8:

- Reference: standard 1µm CMOS process
- External metallization: After the MOVPE of the III/V stack a different metal system was used with regards to the reference CMOS process. Some wafers were processed only with the changed metallization.

- External metallization and MOVPE: complete LED processing and metallization.

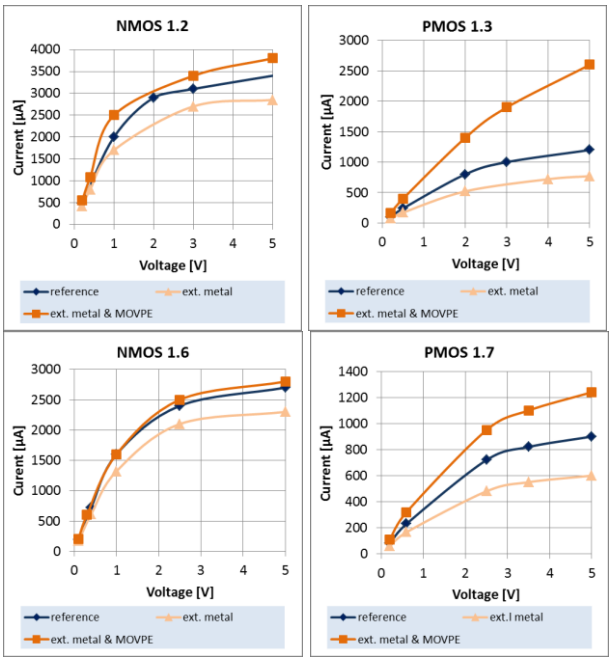

Figure 8: CMOS output characteristics of n-channel and p-channel devices with different gate length, each device measured with Vgs=5V at a width of 20µm

A picture of the 750µm*200µm LEDs is given in Figure 9. There is no indication for a limitation in decreasing the LED area. One large contact is on top of the LED stack, the second n-contact was realized on silicon adjacent to the LED. The forward current voltage characteristics and the related optical output power of a 1000nm LED are shown in Figure 10.
Not only proper light emission of the forward biased LED stack with wavelengths tuneable between 850 nm and 1115 nm but also optocoupler operation was demonstrated, Figure 11: A second LED device, manually placed adjacent to the first one, was used for light detection. With an input signal of 4V an output signal of about 25mV was measured.

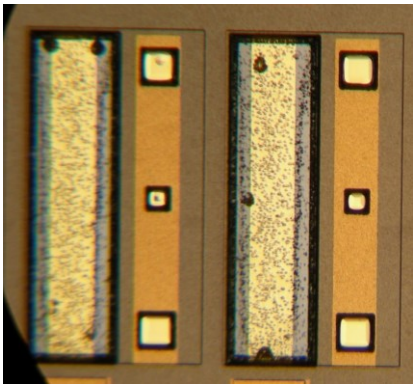

Figure 9: optical microscope picture of a LED stack

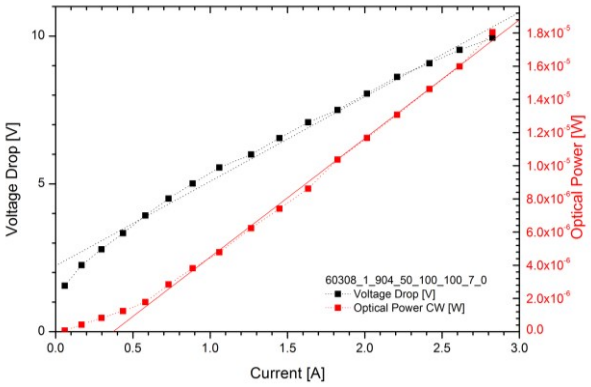

Figure 10: Forward current-voltage characteristic of the LED and the optical power of the LED

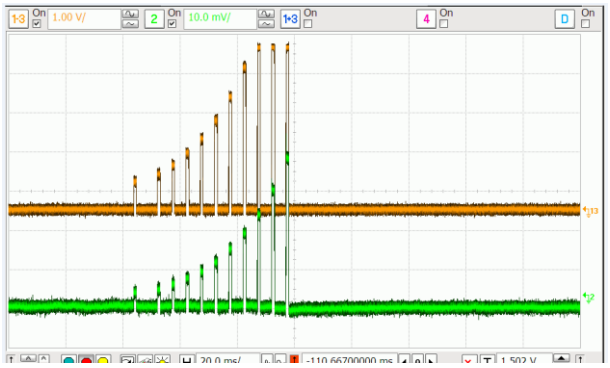

Figure 11: two LEDs arranged as optocoupler, input (top, orange; 1V/div) and output (bottom, green, 10mV/div)

Discussion

A significant impact on the CMOS performance was already seen with a change in the metallization system. Saturation currents are significantly reduced for the n-channel as well as for the p-channel device when changing the metallization. The MOVPE processing of the III/V LED stack itself is below 600°C [6] and should be uncritical for the CMOS device performance. Nevertheless one de-oxidation step (about 1000°C, 20min, [7]) was done which causes additional under diffusion of the CMOS source drain implants leading to a shorter channel length and increased saturation currents. Especially critical is the PMOS with shortest allowed channel length of 1.3µm.
Nevertheless working CMOS devices could be demonstrated.
Several advantages of this topology (bidirectional communication between the high and the low voltage side, galvanic separation) have to be weighed versus a quite complex process architecture.

CONCLUSION

A comparison of the devices developed for the different level shifting approaches is shown in Table 3.

Device	900V DMOS	900V Capacitor, ~1.5pF (0.3pF)	Inductor, 20 windings	LED
Size	735µm * 735µm	200µm * 600µm	350µm * 350µm	200µm * 760µm
Area	0.53mm²	0.15mm² (0.03mm²)	0.12mm²	0.15mm² (0.05mm²)
Die #	6	6	3	3 (6)
Comments	Parasitic capa-citances	Parasitic capa-citances	>10MHz and/or steep signal slope	Galvanic separation <-> complex process

Table 3: Comparison of different level shifter structures.

With footprints of only 0.15mm² and less, the investigated alternative level shifting devices are much smaller than the conventional 900V transistor but with several pros and cons which need to be considered.
The die count in Table 3 is based on the usage of a differential signal transfer but without a feed-back loop from hi to lo. An advantage of the inductive coil transformer is that "set" and "reset" can be done by the same coil.
The driver of the high voltage shifting device has to generate adequate signals for the different shifting devices: In case of an optical shifter a short high current needle is driven into a LED. In case of the inductive shifter a pulse with very steep edges is driven into the primary coil. In case of the capacitive and DMOS shifter the signal is split into complementary pulse signals with adequate current capability, voltage level and timing. Also the high side flip flop has to be matched to the different transmitted signals: In case of the optical and inductive shifter the flip flop has to be very fast to sense short and low amplitude signals. In case of the capacitive and DMOS shifter the flip flop must not alter its state at occurrence of common mode failure signals induced into the high voltage shifting path during commutation of the external IGBTs.

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