Chemnitz University of Technology
Chair of Digital Signal Processing
and Circuit Technology

Research Project/ Bachelor Thesis

Ethernet Core for FPGA

Description

Digital signal processing applications at high data rates makes FPGAs mandatory. The data to be processed needs to be sent to the FPGA and back through an Ethernet connection. There are many IP-Cores available but on the FPGA different interfaces are possible. This interface needs to be compatible with the rest of the FPGA-implementation. Here a research is necessary to get an overview of the available cores and their interfaces. The task includes an analysis of the interfaces, their functionality and the compatibility towards the final application.

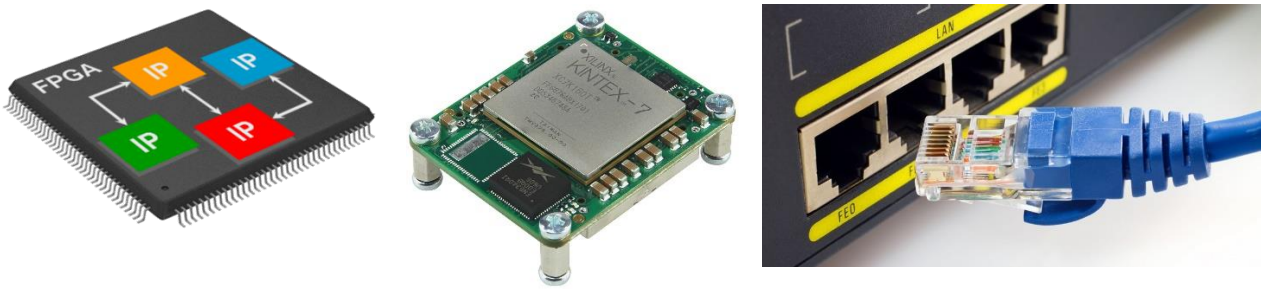

Figure 1: FPGA Ethernet Core

The student's work isn't limited to this work but should at least include the following steps:

- Create an overview of the available IP-cores
- Analysis of the interfaces
- Comparison with the existing interface of the application (CHDR/RFNoC)
- Find a possibility to connect the core to the application

Recommended experience

- Fundamental knowledge of communication systems
- Basic knowledge of bus systems especially Ethernet
- Basic understanding in FPGA and HDL (preferably Verilog)

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