| **Number** | **Category** | **Units** | **Description** | **Pins** |
| --- | --- | --- | --- | --- |
| 4000 | Logic Gates | 2 | Dual 3-input NOR gate + 1 [NOT gate](https://en.wikipedia.org/wiki/Inverter_%28logic_gate%29) | 14 |
| 4001 | Logic Gates | 4 | Quad 2-input [NOR gate](https://en.wikipedia.org/wiki/NOR_gate) | 14 |
| 4002 | Logic Gates | 2 | Dual 4-input [NOR gate](https://en.wikipedia.org/wiki/NOR_gate) | 14 |
| 4006 | Shift Registers | 1 | 18-stage [shift register](https://en.wikipedia.org/wiki/Shift_register) | 14 |
| 4007 | - | 2 | Dual complementary transistor pair + 1 [NOT gate](https://en.wikipedia.org/wiki/Inverter_%28logic_gate%29) | 14 |
| 4008 | Adders | 1 | 4-bit binary full [adder](https://en.wikipedia.org/wiki/Adder_%28electronics%29) | 16 |
| 4009 | Buffers | 6 | Hex inverting [buffer](https://en.wikipedia.org/wiki/Buffer_amplifier) (replaced by 4049) | 16 |
| 4010 | Buffers | 6 | Hex non-inverting [buffer](https://en.wikipedia.org/wiki/Buffer_amplifier) (replaced by 4050) | 16 |
| 4011 | Logic Gates | 4 | Quad 2-input [NAND gate](https://en.wikipedia.org/wiki/NAND_gate) | 14 |
| 4012 | Logic Gates | 2 | Dual 4-input [NAND gate](https://en.wikipedia.org/wiki/NAND_gate) | 14 |
| 4013 | Flip-Flops | 2 | Dual D-type [flip-flop](https://en.wikipedia.org/wiki/Flip-flop_%28electronics%29) | 14 |
| 4014 | Shift Registers | 1 | 8-stage [shift register](https://en.wikipedia.org/wiki/Shift_register) | 16 |
| 4015 | Shift Registers | 2 | Dual 4-stage [shift register](https://en.wikipedia.org/wiki/Shift_register) | 16 |
| 4016 | Analog Switches | 4 | Quad [bilateral switch](https://en.wikipedia.org/wiki/Analog_switch) | 14 |
| 4017 | Counters | 1 | Decade counter with 10 decoded outputs (5-stage [Johnson counter](https://en.wikipedia.org/wiki/Johnson_counter)) | 16 |
| 4018 | Counters | 1 | Presettable divide-by-N counter | 16 |
| 4019 | Logic Gates | 4 | Quad AND/OR select [gate](https://en.wikipedia.org/wiki/Gate) | 16 |
| 4020 | Counters | 1 | 14-stage [binary ripple counter](https://en.wikipedia.org/wiki/Counter_%28digital%29) | 16 |
| 4021 | Shift Registers | 1 | 8-stage [shift register](https://en.wikipedia.org/wiki/Shift_register) | 16 |
| 4022 | Counters | 1 | Octal counter with 8 decoded outputs (4-stage Johnson counter) | 16 |
| 4023 | Logic Gates | 3 | Triple 3-input [NAND gate](https://en.wikipedia.org/wiki/NAND_gate) | 14 |
| 4024 | Counters | 1 | 7-stage [binary ripple counter](https://en.wikipedia.org/wiki/Counter_%28digital%29) | 14 |
| 4025 | Logic Gates | 3 | Triple 3-input [NOR gate](https://en.wikipedia.org/wiki/NOR_gate) | 14 |
| 4026 | 7-Segment Decoders | 1 | Decade counter with decoded [7-segment display outputs](https://en.wikipedia.org/wiki/Seven-segment_display) and display enable | 16 |
| 4027 | Flip-Flops | 2 | Dual J-K master-slave flip-flop | 16 |
| 4028 | Multiplexers | 1 | BCD to decimal (1-of-10) decoder | 16 |
| 4029 | Counters | 1 | Presettable up/down counter, binary or BCD-decade | 16 |
| 4030 | Logic Gates | 4 | Quad [XOR](https://en.wikipedia.org/wiki/XOR) gate (replaced by 4070) | 14 |
| 4031 | Shift Registers | 1 | 64-stage [shift register](https://en.wikipedia.org/wiki/Shift_register) | 16 |
| 4032 | Adders | 3 | Triple serial adder | 20 |
| 4033 | 7-Segment Decoders | 1 | Decade counter with decoded 7-segment display outputs and ripple blanking | 16 |
| 4034 | Registers | 1 | 8-stage bidirectional parallel/serial input/output register | 24 |
| 4035 | Shift Registers | 1 | 4-stage parallel-in/parallel-out shift register | 16 |
| 4038 | Adders | 3 | Triple serial adder | 20 |
| 4040 | Counters | 1 | 12-stage binary ripple counter | 16 |
| 4041 | Buffers | 4 | Quad true/complement [buffer](https://en.wikipedia.org/wiki/Buffer_amplifier) | 14 |
| 4042 | Latches | 4 | Quad D-type latch | 16 |
| 4043 | Latches | 4 | Quad NOR [R/S latch](https://en.wikipedia.org/wiki/Latch_%28electronics%29) with [tri-state](https://en.wikipedia.org/wiki/Three-state_logic) outputs | 16 |
| 4044 | Latches | 4 | Quad NAND R/S latch with tri-state outputs | 16 |
| 4045 | Counters | 1 | 21-stage counter | 16 |
| 4046 | PLL | 1 | [Phase-locked loop](https://en.wikipedia.org/wiki/Phase-locked_loop) with [VCO](https://en.wikipedia.org/wiki/Voltage-controlled_oscillator) | 16 |
| 4047 | Multivibrators | 1 | [Monostable](https://en.wikipedia.org/wiki/Monostable)/[astable](https://en.wikipedia.org/wiki/Astable) [multivibrator](https://en.wikipedia.org/wiki/Multivibrator) | 14 |
| 4048 | Logic Gates | 1 | Multifunctional expandable 8-input gate with tri-state output | 16 |
| 4049 | Buffers | 6 | Hex [buffer](https://en.wikipedia.org/wiki/Buffer_amplifier)/converter (inverting) | 16 |
| 4050 | Buffers | 6 | Hex [buffer](https://en.wikipedia.org/wiki/Buffer_amplifier)/converter (non-inverting) | 16 |
| 4051 | Analog Switches | 1 | 8-channel analog multiplexer/[demultiplexer](https://en.wikipedia.org/wiki/Demultiplexer) | 16 |
| 4052 | Analog Switches | 2 | Dual 4-channel analog multiplexer/demultiplexer | 16 |
| 4053 | Analog Switches | 3 | Triple 2-channel analog multiplexer/demultiplexer | 16 |
| 4054 | LCD Drivers | 1 | 4-segment [LCD](https://en.wikipedia.org/wiki/Liquid_crystal_display) driver | 16 |
| 4055 | LCD Drivers | 1 | BCD to 7-segment decoder/LCD driver with "display-frequency" output | 16 |
| 4056 | LCD Drivers | 1 | BCD to 7-segment decoder/LCD driver with strobed-latch function | 16 |
| 4059 | Counters | 1 | Programmable divide-by-N counter | 24 |
| 4060 | Counters | 1 | 14-stage binary ripple counter and [oscillator](https://en.wikipedia.org/wiki/Oscillator) | 16 |
| 4062 |  | ? | Logic dual 3 majority gate |  |
| 4063 | Comparators | 1 | 4-bit [digital comparator](https://en.wikipedia.org/wiki/Digital_comparator) | 16 |
| 4066 | Analog Switches | 4 | Quad [analog switch](https://en.wikipedia.org/wiki/Analog_switch) (low "ON" resistance) | 14 |
| 4067 | Analog Switches | 1 | 16-channel analog multiplexer/demultiplexer (1-of-16 switch) | 24 |
| 4068 | Logic Gates | 1 | 8-input [NAND gate](https://en.wikipedia.org/wiki/NAND_gate) | 14 |
| 4069 | Logic Gates | 6 | Hex inverter | 14 |
| 4070 | Logic Gates | 4 | Quad 2-input [XOR gate](https://en.wikipedia.org/wiki/XOR_gate) | 14 |
| 4071 | Logic Gates | 4 | Quad 2-input [OR gate](https://en.wikipedia.org/wiki/OR_gate) | 14 |
| 4072 | Logic Gates | 2 | Dual 4-input [OR gate](https://en.wikipedia.org/wiki/OR_gate) | 14 |
| 4073 | Logic Gates | 3 | Triple 3-input [AND gate](https://en.wikipedia.org/wiki/AND_gate) | 14 |
| 4075 | Logic Gates | 3 | Triple 3-input [OR gate](https://en.wikipedia.org/wiki/OR_gate) | 14 |
| 4076 | Registers | 4 | Quad D-type register with tri-state outputs | 16 |
| 4077 | Logic Gates | 4 | Quad 2-input [XNOR gate](https://en.wikipedia.org/wiki/XNOR_gate) | 14 |
| 4078 | Logic Gates | 1 | 8-input [NOR](https://en.wikipedia.org/wiki/NOR_gate)/[OR gate](https://en.wikipedia.org/wiki/OR_gate) | 14 |
| 4081 | Logic Gates | 4 | Quad 2-input [AND gate](https://en.wikipedia.org/wiki/AND_gate) | 14 |
| 4082 | Logic Gates | 2 | Dual 4-input [AND gate](https://en.wikipedia.org/wiki/AND_gate) | 14 |
| 4085 | Logic Gates | 2 | Dual 2-wide, 2-input AND/OR invert (AOI) | 14 |
| 4086 | Logic Gates | ? | Expandable 4-wide, 2-input AND/OR invert (AOI) | 14 |
| 4089 | Rate Multipliers | 1 | [Binary rate multiplier](https://en.wikipedia.org/w/index.php?title=Binary_rate_multiplier&action=edit&redlink=1) | 16 |
| 4093 | Logic Gates | 4 | Quad 2-input [Schmitt trigger](https://en.wikipedia.org/wiki/Schmitt_trigger) NAND gate | 14 |
| 4094 | Shift Registers | 1 | 8-stage shift-and-store bus | 16 |
| 4095 | Flip-Flops | 1 | Gated J-K flip-flop (non-inverting) | 20 |
| 4096 | Flip-Flops | 1 | Gated J-K flip-flop (inverting and non-inverting) | 20 |
| 4097 | Analog Switches | 1 | Differential 8-channel analog multiplexer/demultiplexer | 24 |
| 4098 | Multivibrators | 2 | Dual one-shot [monostable](https://en.wikipedia.org/wiki/Monostable) | 16 |
| 4099 | Latches | 1 | 8-bit addressable latch | 16 |
| 4104 | Translators | 4 | Quad low-to-high voltage translator with tri-state outputs | 16 |
| 4106 | Logic Gates | 6 | Hex [Schmitt trigger](https://en.wikipedia.org/wiki/Schmitt_trigger) | 14 |
| 4160 | Counters | 1 | Decade counter with asynchronous clear |  |
| 4161 | Counters | 1 | 4-bit binary counter with asynchronous clear |  |
| 4162 | Counters | 1 | Decade counter with synchronous clear |  |
| 4163 | Counters | 1 | 4-bit binary counter with synchronous clear |  |
| 4174 | Flip-Flops | 6 | Hex D-type [Flip-Flop](https://en.wikipedia.org/wiki/Flip-flop_%28electronics%29) | 16 |
| 4175 | Flip-Flops | 4 | Quad D-type flip-flop | 16 |
| 4192 | Counters | 1 | Presettable up-down counter |  |
| 4490 |  | 6 | Hex contact bounce eliminator | 16 |
| [4500](https://en.wikipedia.org/wiki/Motorola_MC14500B) |  | 1 | Industrial control unit |  |
| 4502 |  | 6 | Hex inverting [buffer](https://en.wikipedia.org/wiki/Buffer_amplifier) (tri-state) | 16 |
| 4503 |  | 6 | Hex non-inverting [buffer](https://en.wikipedia.org/wiki/Buffer_amplifier) with tri-state outputs | 16 |
| 4504 | Translators | 6 | Hex voltage level shifter for TTL-to-CMOS or CMOS-to-CMOS operation | 16 |
| 4505 |  | 1 | 64-bit, 1-bit per word random access memory (RAM) | 14 |
| 4508 | Latches | 2 | Dual 4-bit latch with tri-state outputs | 24 |
| 4510 | Counters | 1 | Presettable 4-bit BCD up/down counter | 16 |
| 4511 | 7-Segment Decoders | 1 | BCD to 7-segment latch/decoder/driver | 16 |
| 4512 | Multiplexers | 1 | 8-input multiplexer (data selector) with tri-state output | 16 |
| 4513 | 7-Segment Decoders | 1 | BCD to 7-segment latch/decoder/driver (4511 plus ripple blanking) | 18 |
| 4514 | Multiplexers | 1 | 1-of-16 decoder/demultiplexer active HIGH output | 24 |
| 4515 | Multiplexers | 1 | 1-of-16 decoder/demultiplexer active LOW output | 24 |
| 4516 | Counters | 1 | Presettable 4-bit binary up/down counter | 16 |
| 4517 | Shift Registers | 2 | Dual 64-stage shift register | 16 |
| 4518 | Counters | 2 | Dual BCD up counter | 16 |
| 4519 |  | 4 | Quad 2-input multiplexer (data selector) | 16 |
| 4520 | Counters | 2 | Dual 4-bit binary up counter | 16 |
| 4521 |  | 1 | 24-stage frequency divider |  |
| 4522 |  | 1 | Programmable BCD divide-by-N counter |  |
| 4526 | Counters | 1 | Programmable 4-bit binary down counter |  |
| 4527 |  | 1 | BCD rate multiplier |  |
| 4528 |  | 2 | Dual [retriggerable monostable](https://en.wikipedia.org/wiki/Retriggerable_monostable) multivibrator with reset |  |
| 4529 |  | 2 | Dual 4-channel analog data selector/multiplexer |  |
| 4530 |  | 2 | Dual 5-input majority logical gate |  |
| 4531 |  | 1 | 12-bit parity tree |  |
| 4532 | Multiplexers | 1 | 8-bit [priority encoder](https://en.wikipedia.org/wiki/Priority_encoder) |  |
| 4536 | Timers | 1 | Programmable timer |  |
| 4538 |  | 2 | Dual retriggerable precision monostable multivibrator | 16 |
| 4539 |  | 2 | Dual 4-input multiplexer |  |
| 4541 | Timers | 1 | Programmable timer |  |
| 4543 | 7-Segment Decoders | 1 | BCD to 7-segment latch/decoder/driver with phase input |  |
| 4549 |  | 1 | Successive approximation registers |  |
| 4551 | Analog Switches | 4 | Quad 2-channel analog multiplexer/demultiplexer |  |
| 4553 | Counters | 1 | 3-digit BCD counter |  |
| 4555 | Multiplexers | 2 | Dual 1-of-4 decoder/demultiplexer active HIGH output |  |
| 4556 | Multiplexers | 2 | Dual 1-of-4 decoder/demultiplexer active LOW output |  |
| 4557 | Shift Registers | 1 | 1-to-64 bit variable length [shift register](https://en.wikipedia.org/wiki/Shift_register) |  |
| 4558 | 7-Segment Decoders | 1 | BCD to 7-segment decoder (enable, RBI and provides active–high output) |  |
| 4559 |  | 1 | Successive approximation registers |  |
| 4560 | Adders | 1 | [NBCD adder](https://en.wikipedia.org/w/index.php?title=NBCD_adder&action=edit&redlink=1) |  |
| 4562 |  | 1 | 128–bit static shift register |  |
| 4566 |  | 1 | Industrial [time-base generator](https://en.wikipedia.org/w/index.php?title=Time-base_generator&action=edit&redlink=1) |  |
| 4569 | Counters | 1 | Programmable divide-By-N, dual 4-Bit binary/BCD down counter |  |
| 4572 | Logic Gates | 6 | Hex gate: quad [NOT](https://en.wikipedia.org/wiki/NOT_gate), single [NAND](https://en.wikipedia.org/wiki/NAND_gate), single [NOR](https://en.wikipedia.org/wiki/NOR_gate) |  |
| 4583 |  | 2 | Dual [Schmitt trigger](https://en.wikipedia.org/wiki/Schmitt_trigger) |  |
| 4584 | Logic Gates | 6 | Hex inverting [Schmitt trigger](https://en.wikipedia.org/wiki/Schmitt_trigger) |  |
| 4585 |  | 1 | 4-bit [digital comparator](https://en.wikipedia.org/wiki/Digital_comparator) |  |
| 4724 |  | 1 | 8-bit addressable latch |  |
| 4750 |  | 1 | [Frequency synthesizer](https://en.wikipedia.org/wiki/Frequency_synthesizer) |  |
| 4751 |  | 1 | Universal divider |  |
| 4794 |  | 1 | 8-stage shift-and-store register [LED](https://en.wikipedia.org/wiki/LED) driver |  |
| 4894 |  | 1 | 12-stage shift-and-store register LED driver |  |
| 4938 |  | 2 | Dual retriggerable precision [monostable multivibrator](https://en.wikipedia.org/w/index.php?title=Monostable_multivibrator&action=edit&redlink=1) with reset |  |
| 4952 |  | 1 | 8-channel analog multiplexer/demultiplexer |  |
| 40098 | Buffers | 6 | 3-state inverting buffer | 16 |
| 40100 | Shift Registers | 1 | 32-bit left/right [shift register](https://en.wikipedia.org/wiki/Shift_register) |  |
| 40101 |  | 1 | 9-bit parity generator/checker |  |
| 40102 | Counters | 1 | Presettable 2-decade BCD down counter |  |
| 40103 | Counters | 1 | Presettable 8-bit binary down counter |  |
| 40104 |  | 1 | 4-bit bidirectional parallel-in/parallel-out shift register (tri-state) |  |
| 40105 |  | 1 | 4-bit x 16 word [FIFO](https://en.wikipedia.org/wiki/FIFO_%28computing_and_electronics%29) register |  |
| 40106 |  | 6 | Hex inverting Schmitt trigger-(NOT gates) |  |
| 40107 |  | 2 | Dual 2-input NAND buffer/driver |  |
| 40108 |  | 1 | 4x4-bit (tri-state) synchronous triple-port register file |  |
| 40109 | Translators | 4 | Quad level shifter |  |
| 40110 |  | 1 | Up/down counter latch decoder driver |  |
| 40116 | Translators | 1 | 8-bit bidirectional CMOS-to-[TTL](https://en.wikipedia.org/wiki/Transistor%E2%80%93transistor_logic) level converter |  |
| 40117 |  | 1 | Programmable dual 4-bit terminator |  |
| 40147 |  | 1 | 10-line to 4-line (BCD) priority encoder |  |
| 40160 | Counters | 1 | Decade counter/asynchronous clear |  |
| 40161 | Counters | 1 | Binary counter/asynchronous clear |  |
| 40162 | Counters | 1 | 4-bit [synchronous](https://en.wikipedia.org/wiki/Synchronization_%28computer_science%29) decade counter with load, reset, and [ripple carry](https://en.wikipedia.org/w/index.php?title=Ripple_carry&action=edit&redlink=1) output |  |
| 40163 | Counters | 1 | 4-bit synchronous binary counter with load, reset, and ripple carry output |  |
| 40174 | Flip-Flops | 6 | Hex D-type [flip-flop](https://en.wikipedia.org/wiki/Flip-flop_%28electronics%29) |  |
| 40175 | Flip-Flops | 4 | Quad D-type [flip-flop](https://en.wikipedia.org/wiki/Flip-flop_%28electronics%29) |  |
| 40181 |  | 1 | 4-bit 16-function [arithmetic logic unit](https://en.wikipedia.org/wiki/Arithmetic_logic_unit) |  |
| 40192 | Counters | 1 | Presettable 4-bit up/down BCD counter |  |
| 40193 | Counters | 1 | Presettable 4-bit up/down binary counter | 16 |
| 40194 | Shift Registers | 1 | 4-bit bidirectional universal [shift register](https://en.wikipedia.org/wiki/Shift_register) |  |
| 40195 | Shift Registers | 1 | 4-bit universal [shift register](https://en.wikipedia.org/wiki/Shift_register) |  |
| 40208 |  | 1 | 4 x 4-bit (tri-state) synchronous triple-port [register file](https://en.wikipedia.org/wiki/Register_file) |  |
| 40240 |  | 8 | Buffer/[Line driver](https://en.wikipedia.org/wiki/Line-level); inverting (tri-state) | 20 |
| 40244 |  | 8 | Buffer/line driver; non-inverting (tri-state) | 20 |
| 40245 |  | 8 | Octal [bus transceiver](https://en.wikipedia.org/w/index.php?title=Bus_transceiver&action=edit&redlink=1); (tri-state) outputs | 20 |
| 40257 |  | 4 | Quad 2-line to 1-line data selector/multiplexer (tri-state) |  |
| 40373 | Latches | 8 | Octal D-type [transparent latch](https://en.wikipedia.org/wiki/Transparent_latch) (tri-state) | 20 |
| 40374 | Flip-Flops | 8 | Octal D-type [flip-flop](https://en.wikipedia.org/wiki/Flip-flop_%28electronics%29); positive-edge trigger (tri-state) | 20 |
| 40501 | Buffers | 6 | Hex [buffer](https://en.wikipedia.org/wiki/Buffer_amplifier)/converter (non-inverting) (pinout variant of 4050)[[8]](https://en.wikipedia.org/wiki/List_of_4000_series_integrated_circuits#cite_note-Schlenzig_1987_Kleincomputer-8) | 16 |
| 40511 | 7-Segment Decoders | 1 | BCD 7-segment decoder, hexadecimal, active high[[8]](https://en.wikipedia.org/wiki/List_of_4000_series_integrated_circuits#cite_note-Schlenzig_1987_Kleincomputer-8) | 16 |
| 45106 |  | 1 | [frequency synthesizer](https://en.wikipedia.org/wiki/Frequency_synthesizer) |  |