Coupling of numerical and symbolic MOR techniques

Fraunhofer Institut
Techno- und
Wirtschaftsmathematik

Workshop
"Model Reduction for Circuit Simulation",
October 30-31, 2008, Hamburg, Germany

Oliver Schmidt

Overview

Motivation for symbolic methods

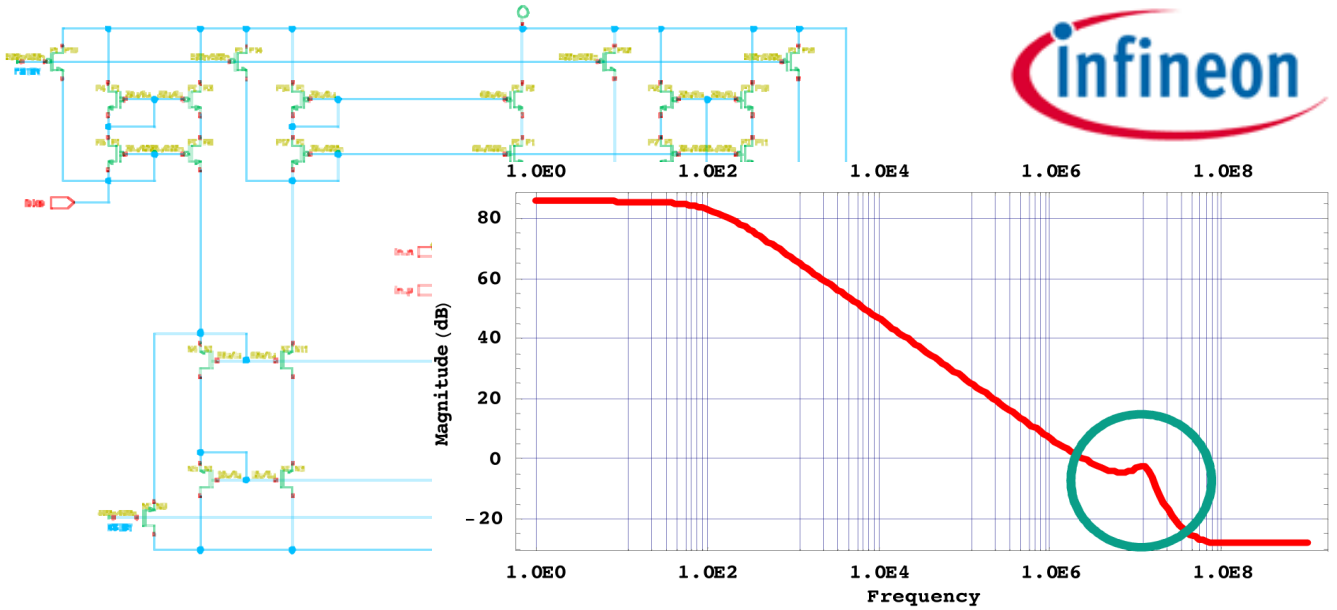
Symbolic techniques

Hierarchic systems

Workflow for exploitation of the hierarchy

Symbolic Analysis

Folded-Cascode OpAmp



Problem

What causes resonance at 10 MHz?

Classic approach

parameter variations and numerical simulation
failed because of huge number of parameters

Symbolic analysis

calculation of the transfer function and derivation of a symbolic formula for the resonance frequency

Complexity problem

exact symbolic transfer function consists of more than $5 \cdot 10^{19}$ terms
printed: paper stack with a height of $15 \cdot 10^{9}$ miles
differential order: 19

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SyreNe System Reduction for Nanoscale IC Design

Symbolic Analysis

Folded-Cascode OpAmp

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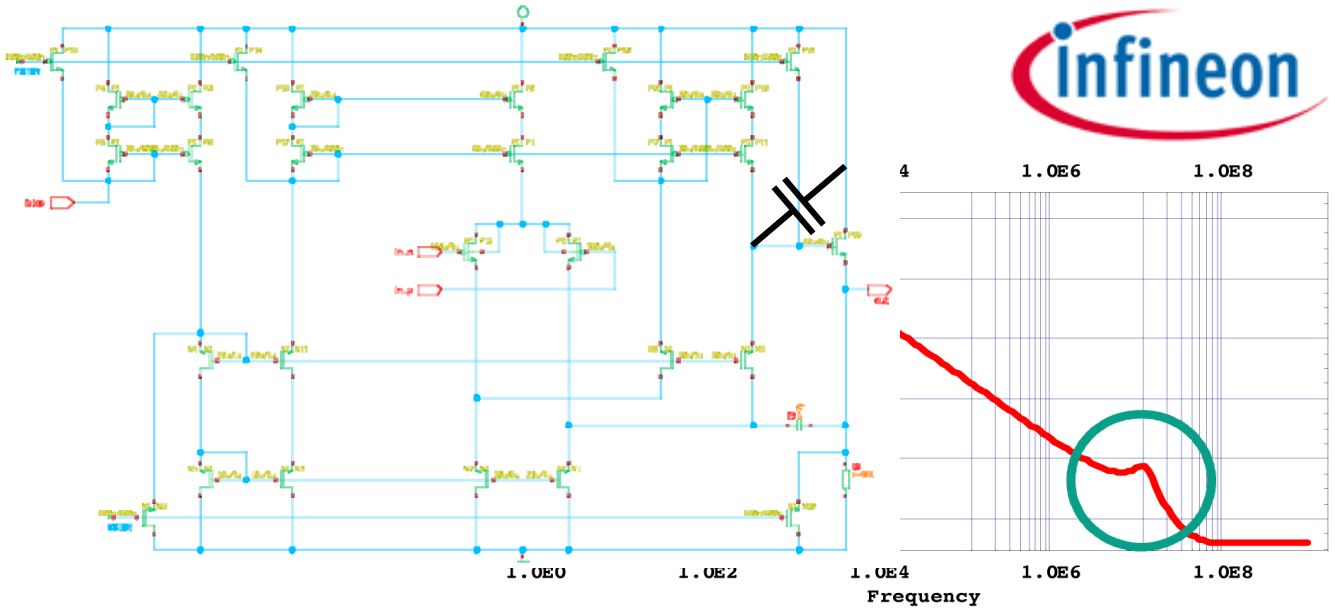

Complexity problem ⇒ symbolic approximation

$$s_p^{1,2} == -\frac{(CC0 + CL)\ gm\$MN6}{2\ CC0\ CL} + \frac{\pm\sqrt{Cgs\$MP15\ gm\$MN6\ (Cgs\$MP15\ (CC0 + CL)^2\ gm\$MN6 - 4\ CC0^2\ CL\ gm\$MP15)}}{2\ CC0\ Cgs\$MP15\ CL}$$

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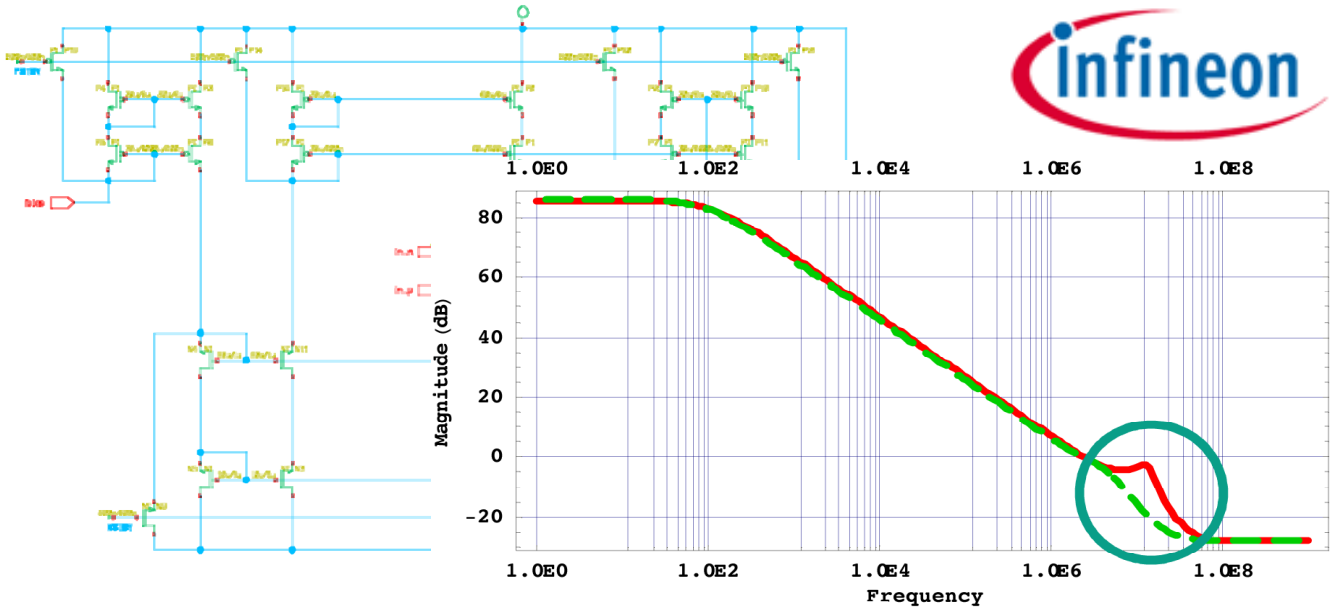

Complexity problem ⇒ symbolic approximation

$$s_p^{1,2} == -\frac{(CC0 + CL)\ gm\$MN6}{2\ CC0\ CL} \pm \frac{\sqrt{Cgs\$MP15\ gm\$MN6\ (Cgs\$MP15\ (CC0 + CL)^2\ gm\$MN6 - 4\ CC0^2\ CL\ gm\$MP15)}}{2\ CC0\ Cgs\$MP15\ CL}$$

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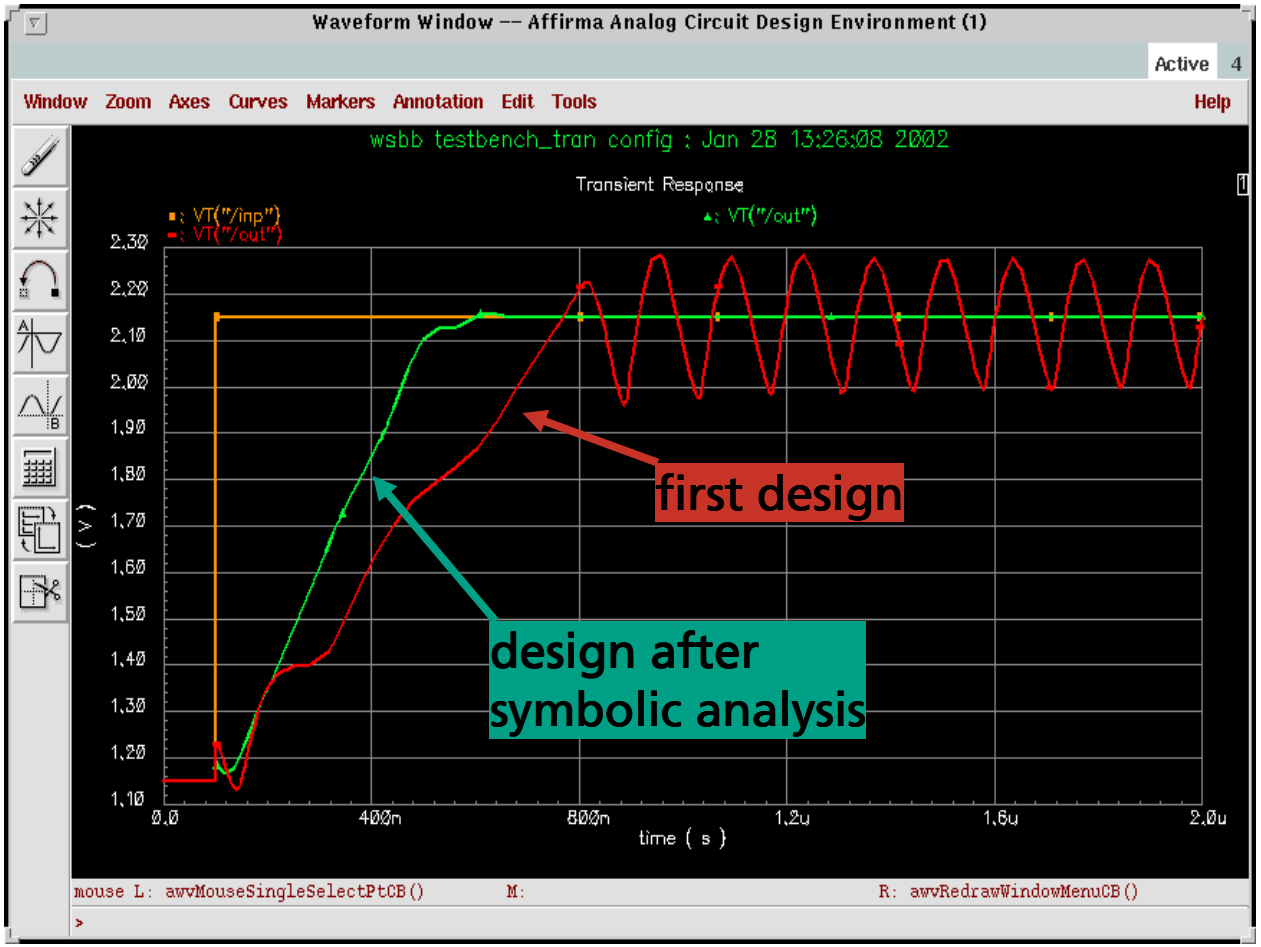
SyreNe System Reduction for Nanoscale IC Design

Numerical Validation



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SyreNe System Reduction for Nanoscale IC Design

Overview

Motivation for symbolic methods

Symbolic techniques

Hierarchic systems

Workflow for exploitation of the hierarchy

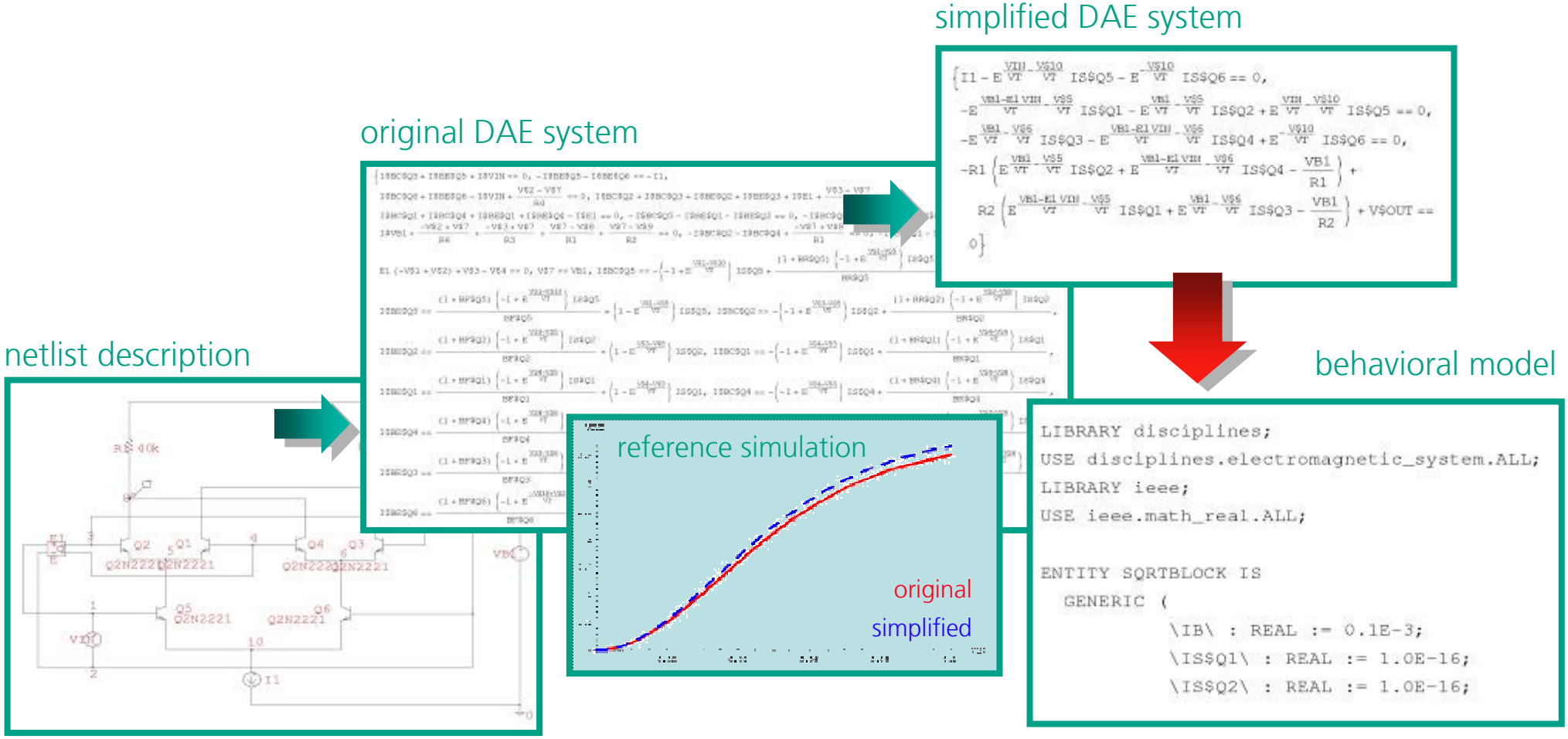
Nonlinear Symbolic Analysis

simplified DAE system

original DAE system

netlist description

behavioral model



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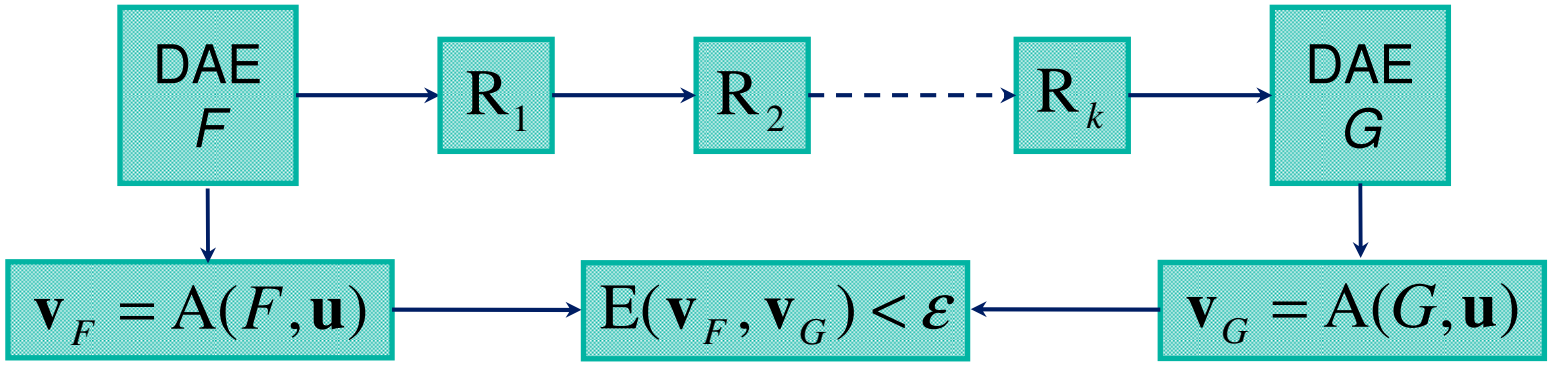
Symbolic Model Reduction



- **Specifications**
  - inputs *u*, outputs *v*
  - numerical analyses **A**
- **Error control**
  - error function **E**
  - error bound ε
- **Goal**
  - find DAE system *G* with reduced complexity and defined accuracy
- **Simplification process**
  - iterative application of reduction techniques **R**

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Symbolic Reduction Techniques (1)

$$x = f(y)$$
$$0 = g(x, y)$$

$$0 = g(f(y), y)$$

- **Algebraic manipulation**
  - elimination of variables
  - removal of independent blocks of equations

$$-I\$AC\$D1[t] + C1\,V\$2'[t] == 0$$

$$-AREA\$D1\,(-1 + e^{38.6635\,(V\$1[t]-V\$2[t])})\,IS\$D1 + I\$AC\$D1[t] - GMIN\,(V\$1[t] - V\$2[t]) == 0$$

$$-AREA\$D1\,(-1 + e^{38.6635\,(V\$1[t]-V\$2[t])})\,IS\$D1 + C1\,V\$2'[t] - GMIN\,(V\$1[t] - V\$2[t]) == 0$$

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Symbolic Reduction Techniques (2)

$$f(x) = \begin{cases} f_1(x) & x < a \\ f_2(x) & a \le x \le b \\ f_3(x) & x > b \end{cases} \quad \Rightarrow \quad f(x) = f_2(x) \quad \text{für alle } x$$

- **Branch reduction**
  - detection and removal of unused branches of piecewise-defined functions

```
id$M3 ==
 -If[-vds$M3 ≥ 0, If[1.11022 × 10^-16 - vgs$M3 < 0, 0, If[1.11022 × 10^-16 - vgs$M3 ≤ -vds$M3,
   0.5 KP$M3 (1.11022 × 10^-16 - vgs$M3)^2 W$M3 / L$M3,
   -(1. KP$M3 vds$M3 (1.11022 × 10^-16 + 0.5 vds$M3 - vgs$M3) W$M3 / L$M3)]],
  If[1.11022 × 10^-16 - vgd$M3 < 0, 0, If[1.11022 × 10^-16 - vgd$M3 ≤ vds$M3,
   -(0.5 KP$M3 (1.11022 × 10^-16 - vgd$M3)^2 W$M3 / L$M3),
   -(1. KP$M3 vds$M3 (1.11022 × 10^-16 - 0.5 vds$M3 - vgd$M3) W$M3 / L$M3)]]]

id$M3 == -If[-vds$M3 ≥ 0, 0.5 KP$M3 (1.11022 × 10^-16 - vgs$M3)^2 W$M3 / L$M3, 0]
```

Symbolic Reduction Techniques (3)

$$F_j : \sum_{i=1}^{N} t_i(x) = 0 \quad \Rightarrow \quad G_j : \sum_{\substack{i=1 \\ i \neq k}}^{N} t_i(\tilde{x}) + \kappa = 0$$

- **Term substitution**
  - replace terms of equations with constant value
  - applicable to nested expressions

$$-AREA\$D1\,(-1 + e^{38.6635\,(V\$1[t]-V\$2[t])})\,IS\$D1 + I\$AC\$D1[t] - GMIN\,(V\$1[t] - V\$2[t]) == 0$$

$$-AREA\$D1\,(-1 + e^{38.6635\,(V\$1[t]-V\$2[t])})\,IS\$D1 + I\$AC\$D1[t] - GMIN\,(12. - V\$2[t]) == 0$$

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Symbolic Reduction Techniques (4)

$$F_j : \sum_{i=1}^{N} t_i(x) = 0 \quad \Rightarrow \quad G_j : \sum_{\substack{i=1 \\ i \neq k}}^{N} t_i(\tilde{x}) = 0$$

- **Term reduction**
  - replace terms of equations with zero
  - applicable to nested expressions

$$-AREA\$D1\left(-1+e^{38.6635\,(V\$1[t]-V\$2[t])}\right) IS\$D1 + I\$AC\$D1[t] - GMIN(V\$1[t]-V\$2[t]) == 0$$

$$-AREA\$D1\left(-1+e^{38.6635\,(V\$1[t]-V\$2[t])}\right) IS\$D1 + I\$AC\$D1[t] == 0$$

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Overview

Motivation for symbolic methods

Symbolic techniques

Hierarchic systems

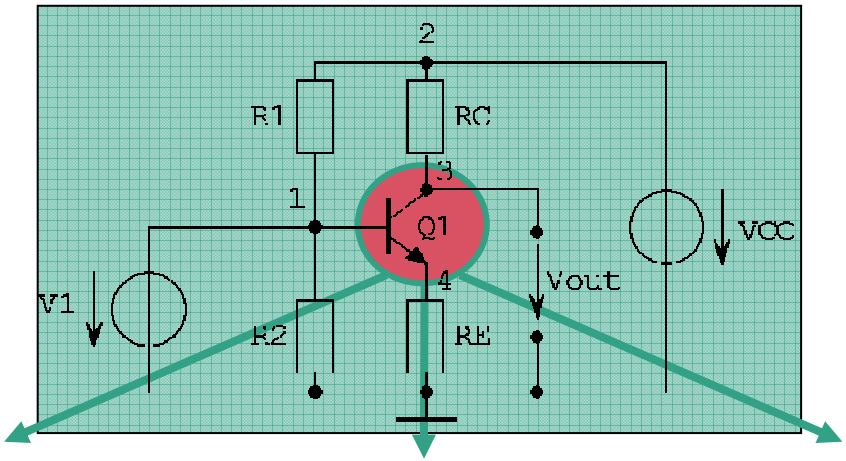
Workflow for exploitation of the hierarchy

New Challenges

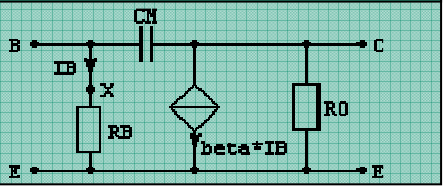
- growing miniaturization of integrated circuits
  → nanoelectronical structures

- increasing integration density of circuit components
  → non-negligible physical effects

↗ Model descriptions based on PDEs!



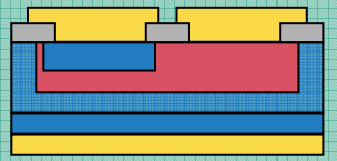
netlist-based model



behavioral model (DAE)

```
b$vbe = "VBE$ac" - b$rb*"IB$ac" - b$RE
b$vbx = "VBC$ac" + b$RCTemp/"AREA"*"IC
b$kqb = 0.5*(1.+LimPower[1.+4.*(
        ("AREA"*b$ISTemp*(Exp[b$Sign*b$v
          + b$Sign*b$vbe*"GMIN") / ("ARE
        + ("AREA"*b$ISTemp*(Exp[b$Sign*b
          + b$Sign*b$vbc*"GMIN") / ("A
```

distributed model (PDE)



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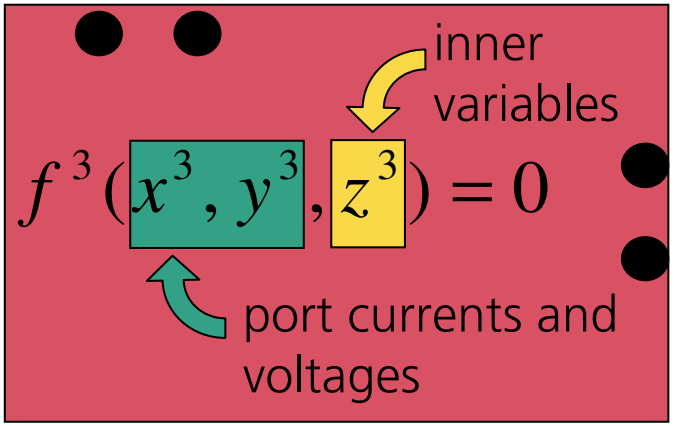
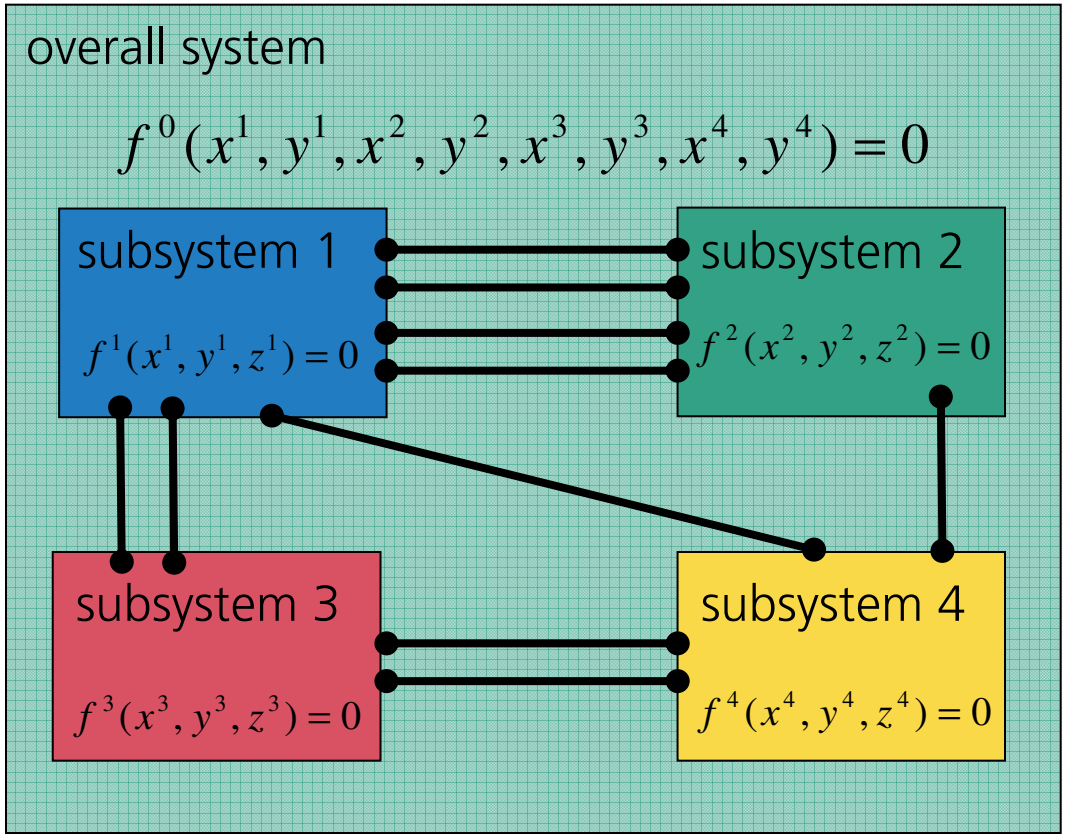
Hierarchic Modelling

→ various components / subsystems using *different mathematical descriptions*, coupled by a topology

currently: "flat" hierarchy
goal: *structure exploitation*





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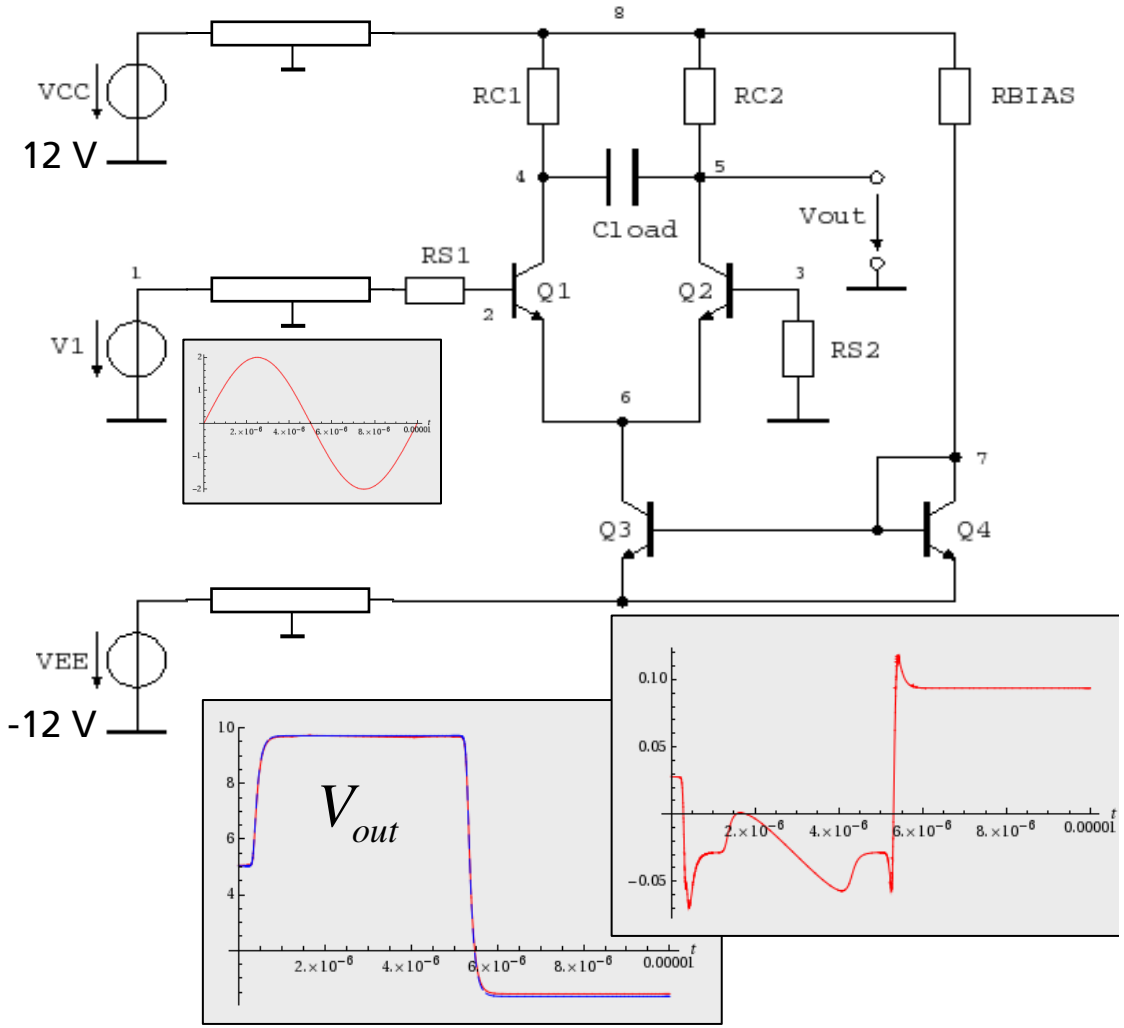
SyreNe System Reduction for Nanoscale IC Design

Differential Amplifier Circuit

- "long distance" transmission lines between sources and components
- discretized PDE model with 20 line segments
- full system:
  167 equations, 645 terms
- symbolic reduction:
  124 equations, 425 terms,
  2% error in magnitude permitted,
  approx. 2 hours and 10 minutes



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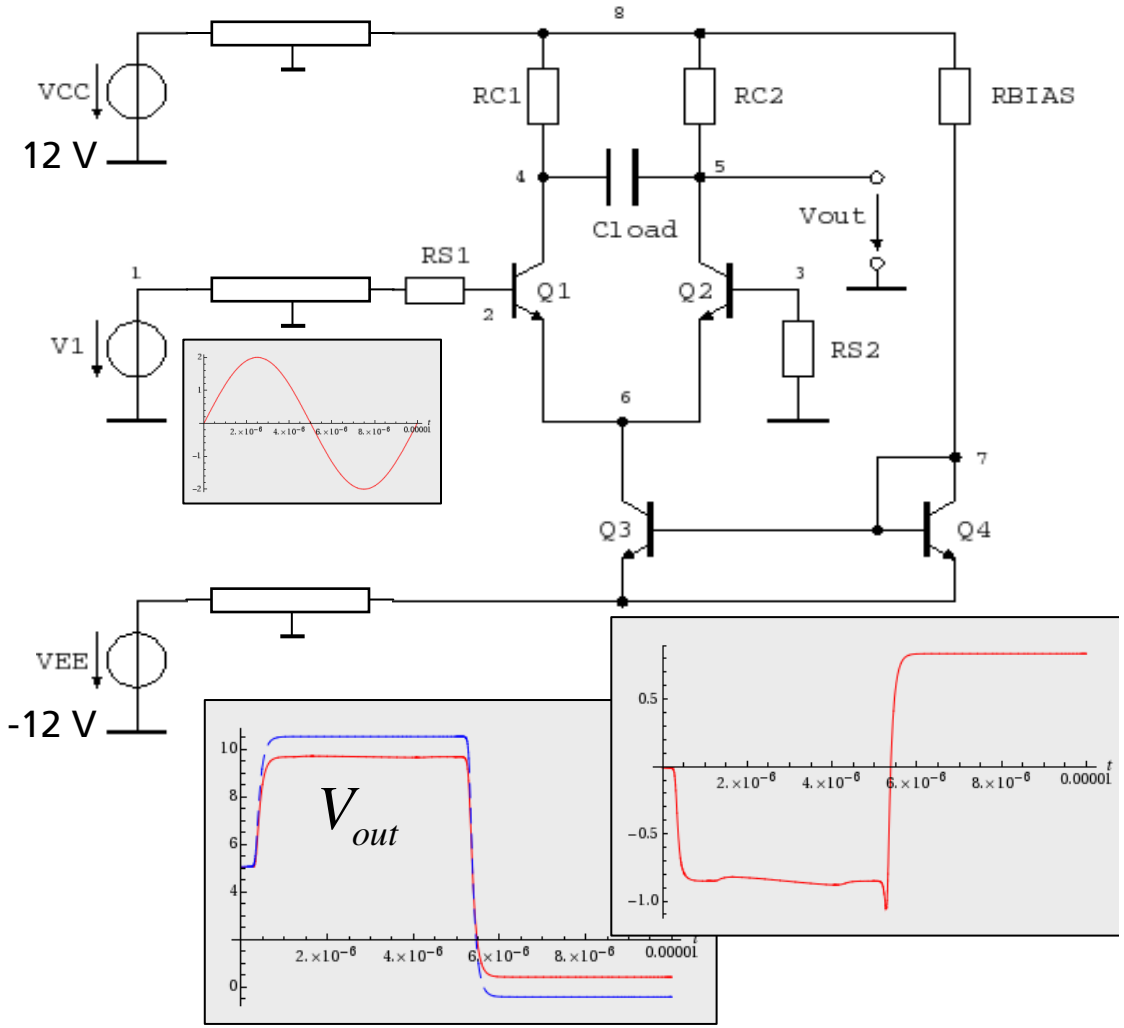
SyreNe
System Reduction for Nanoscale IC Design

Differential Amplifier Circuit

- "long distance" transmission lines between sources and components
- discretized PDE model with 20 line segments
- full system:
  167 equations, 645 terms
- symbolic reduction:
  44 equations, 284 terms,
  10% error in magnitude permitted,
  approx. 2 hours and 10 minutes



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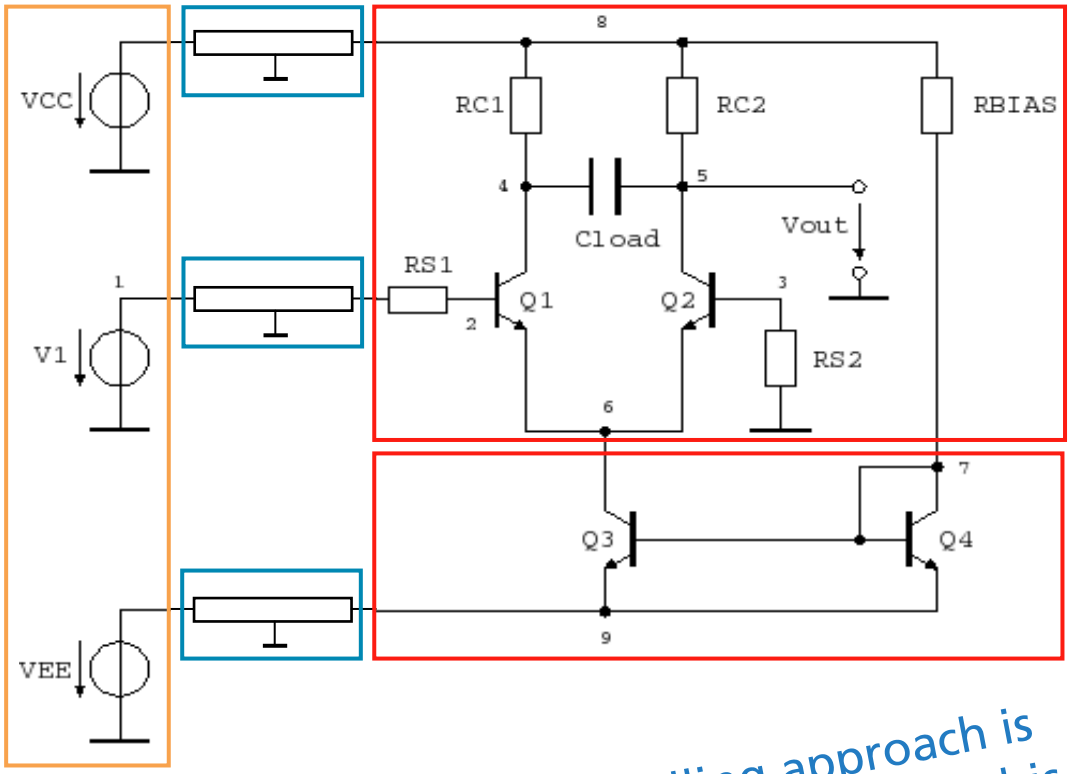
SyreNe
System Reduction for Nanoscale IC Design

Differential Amplifier Circuit

- “intuitive“ hierarchy
- standard graph theoretical methods like MNA / STA lose this information



$$I\$CS\$Q3\$DUT[t] + I\$ES\$Q1\$DUT2[t] + I\$ES\$Q2\$DUT2[t] == 0$$

$$I\$R0\$Rleitung1[t] + \frac{-V\$2\$DUT2[t] + V\$X1[t]}{RS1} == 0$$

$$I\$ES\$Q3\$DUT[t] + I\$ES\$Q4\$DUT[t] + I\$R0\$Rleitung9[t] == 0$$

A modelling approach is aspired that transmits this information into the set of equations!

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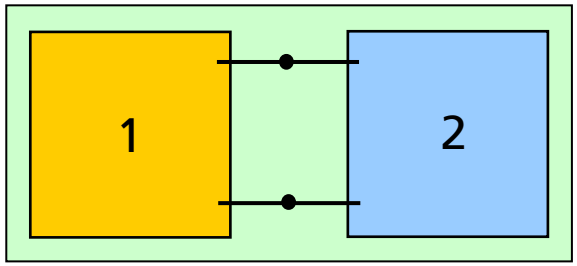
SyreNe System Reduction for Nanoscale IC Design

Macro Modelling

Goal: $f_1(u_1, i_1, x_1) = 0$

$f_2(u_2, i_2, x_2) = 0$

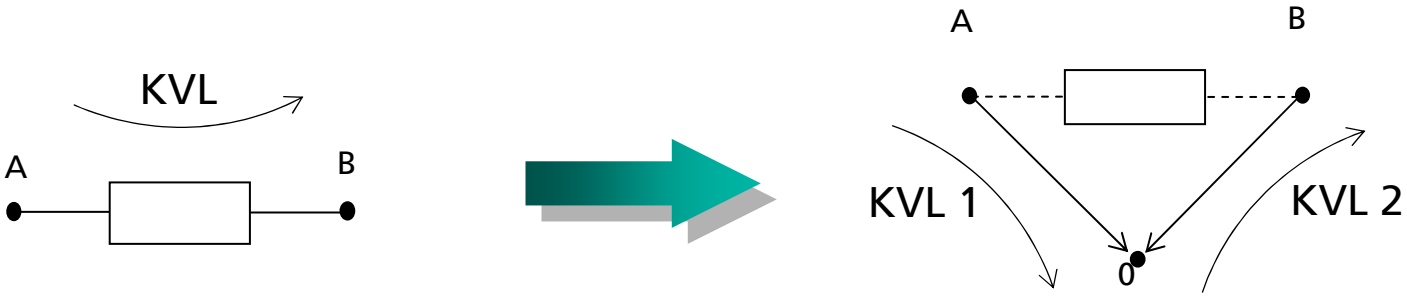


Side effect: $u_1 = u_2$

$i_1 + i_2 = 0$

Idea:

use port currents and voltages
instead of branch magnitudes!



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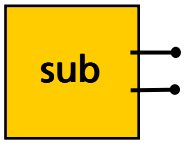
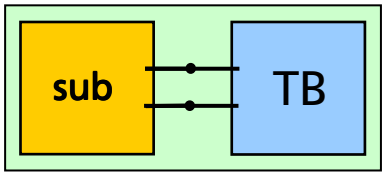
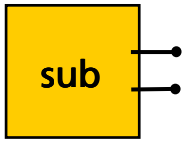
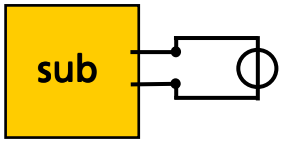
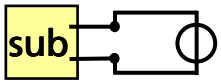
Workflow

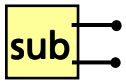
- plug 

in a testbench: 

- record voltages at the ports
- plug a voltage source to 

that delivers exactly the recorded voltages as PWL function
- reduce the circuit 

with appropriate symbolic or numerical methods
- finally remove the voltage source from the reduced circuit 

and receive a reduced subsystem 

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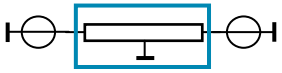
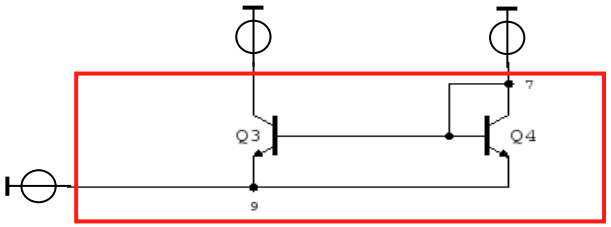
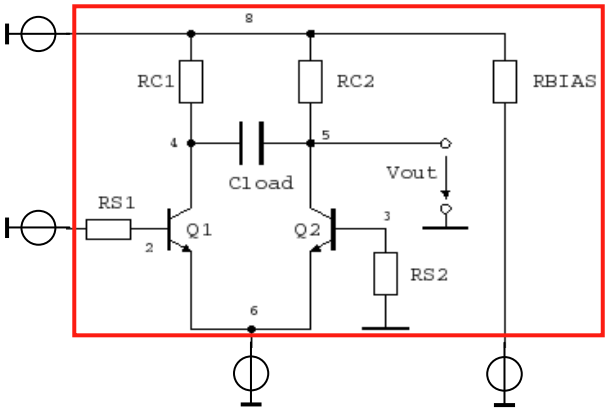
Differential Amplifier Circuit







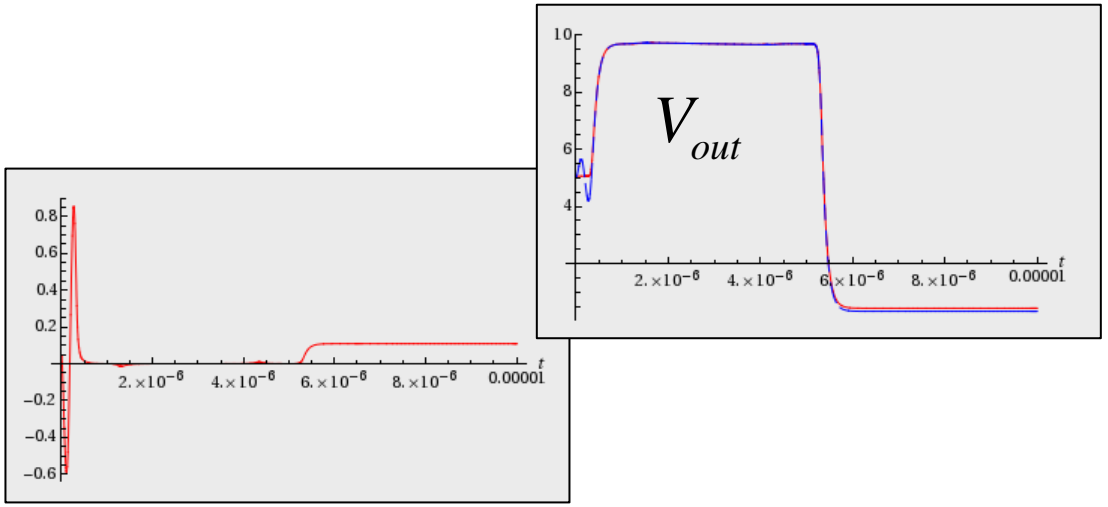
- numerical reduction via state space form and Arnoldi's algorithm within seconds:
  50 ➡ 8 resp. 4 equations
- symbolic reduction within seconds (2% error permitted):
  16 ➡ 9 equations,
  59 ➡ 20 terms
- symbolic reduction within seconds (2% error permitted):
  22 ➡ 13 equations,
  91 ➡ 50 terms

Almost no changes if 10% error is permitted!

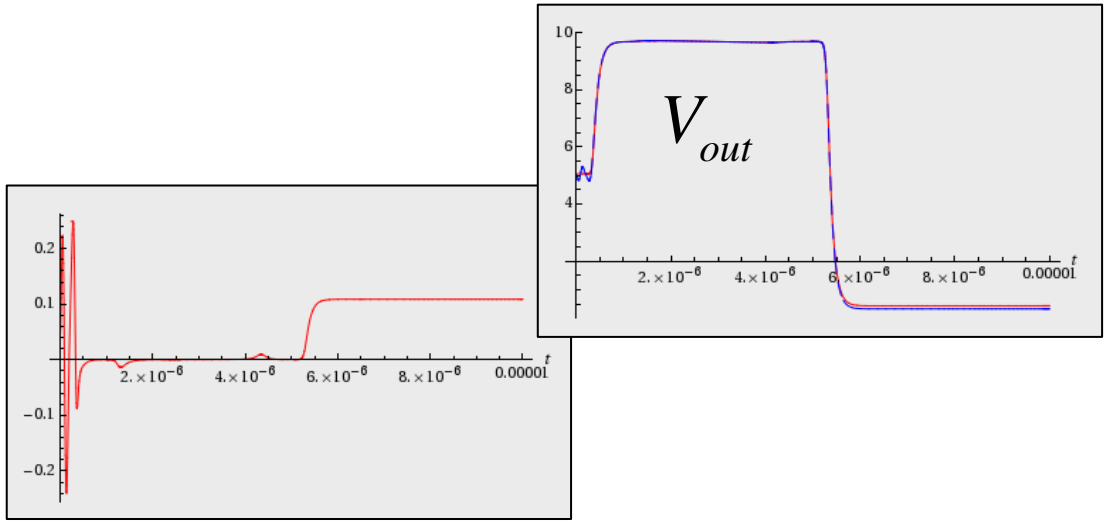
Differential Amplifier Circuit

- plug together all the reduced subsystems:
  167 ⇨ 62 equations,
  645 ⇨ 252 terms

Mostly dependent on the numerical reduction of the conductors!



- by using more modes of conductor1 (12 equations):
  167 ⇨ 66 equations,
  645 ⇨ 396 terms



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SyreNe System Reduction for Nanoscale IC Design

Summary and Outlook

- Proof of concept: Workflow delivers good results for the small circuit example
  → coupling of different subsystems with different mathematical descriptions
  → application of dedicated MOR techniques

- How to get and what is a good segmentation of the overall circuit into subsystems?

- Automatic detection of hierarchical structure.

- Reduce subsystems 1,…,k $\Rightarrow \mathcal{E}_1,\ldots,\mathcal{E}_k$. What about $\mathcal{E}_{ges}$?

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SyreNe System Reduction for Nanoscale IC Design

Thank you for your attention.

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